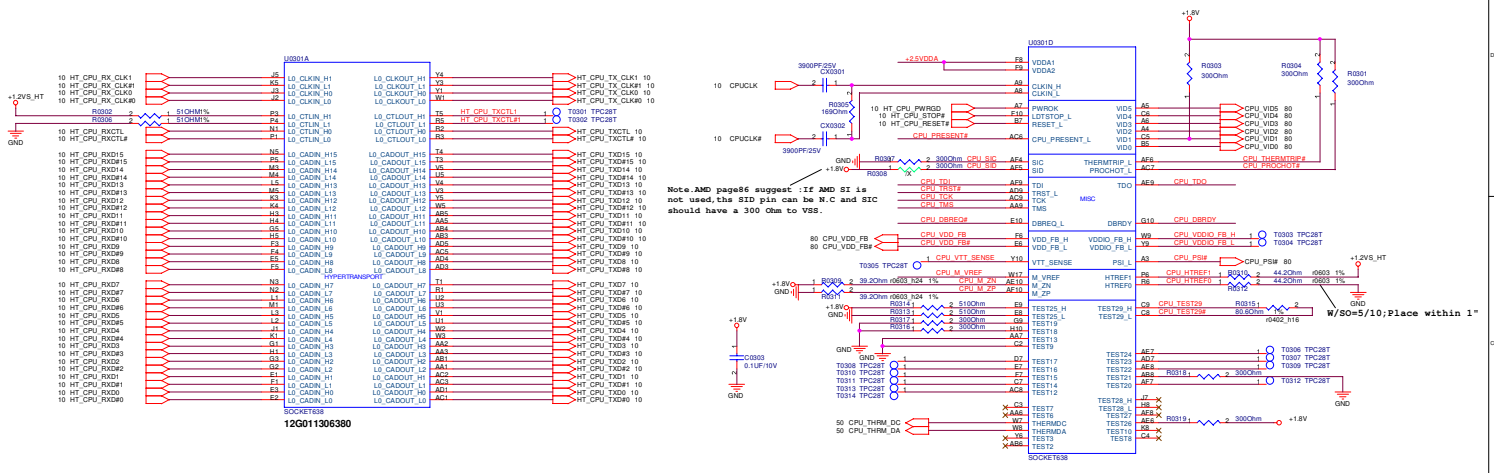
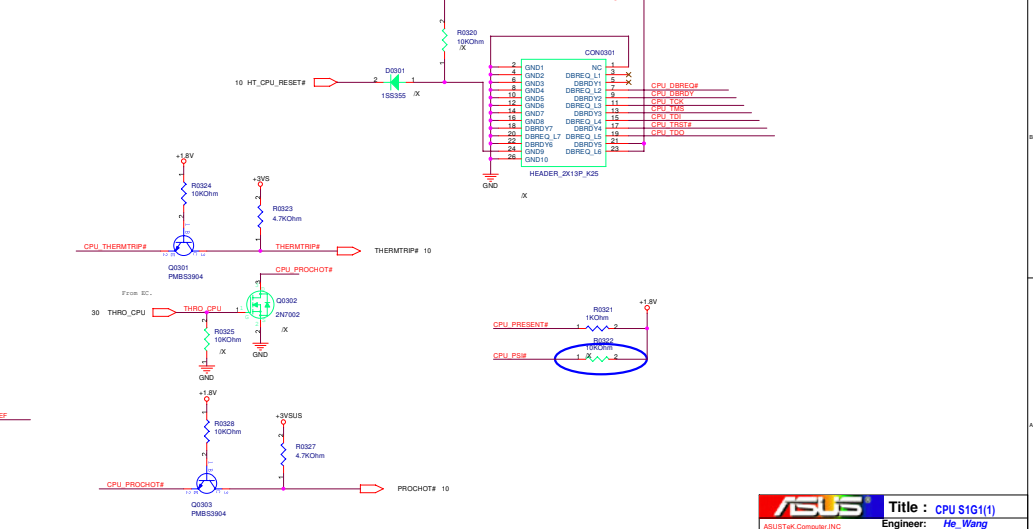
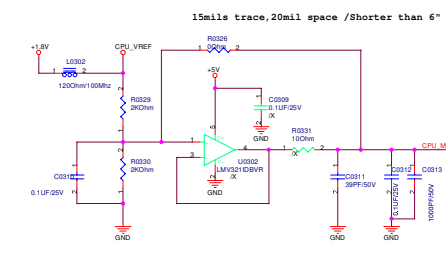
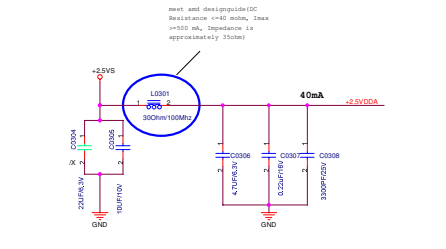
		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 3 of 28	

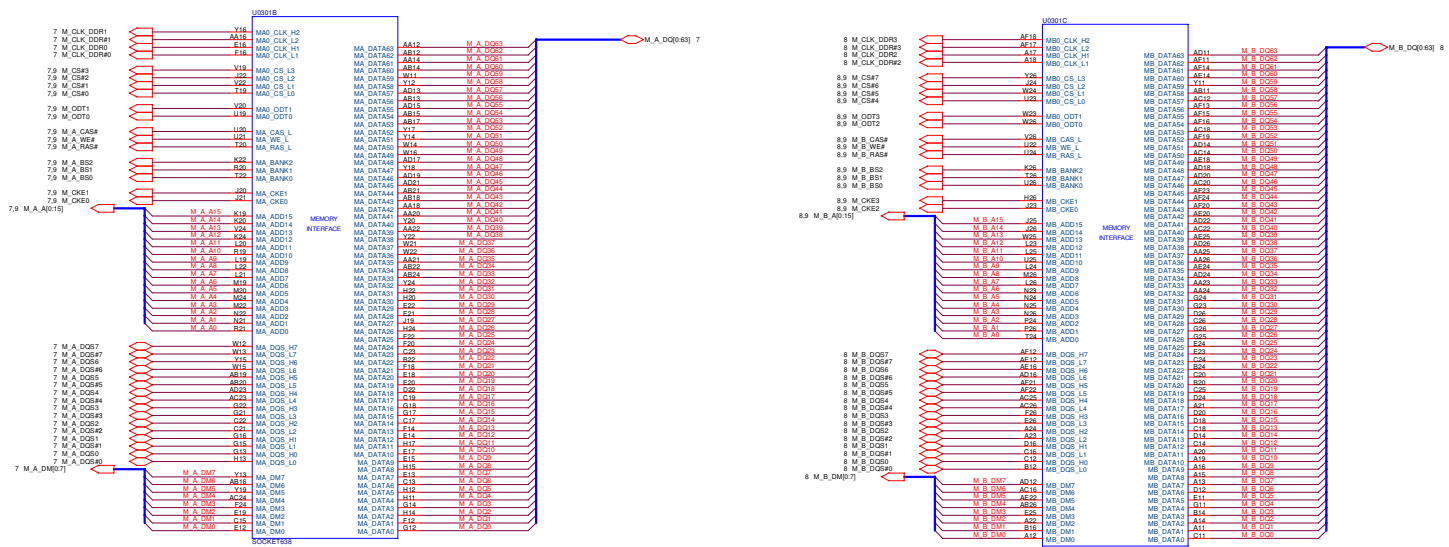
« Kennedy_Zhang »



Note: AMD page 68 suggest if AMD 21 is not used, the SID pin can be N.C. and SIC should have a 300 Ohm to VSS.



« Kennedy_Zhang »



U0001E	U0001B	U0001C	U0001E
T0403 TPC28T	1 CPU_RSVD_MAO_CLK3_P20	RSVD_MAO_CLK_H3	H16 CPU_RSVD_MA_RSTB1_1 O T0402 TPC28T
T0406 TPC28T	1 CPU_RSVD_MAO_CLK0_P18	RSVD_MAO_CLK_L3	H18 CPU_RSVD_MA_RSTB1_2 O T0404 TPC28T
T0401 TPC28T	1 CPU_RSVD_MAO_CLK0_P18	RSVD_MAO_CLK_H0	H3 CPU_RSVD_VIDSTRB0_1 O T0406 TPC28T
T0407 TPC28T	1 CPU_RSVD_MAO_CLK0_P18	RSVD_MAO_CLK_L0	H4 CPU_RSVD_VIDSTRB0_2 O T0408 TPC28T
		RSVD_VIDSTRB0	H6 CPU_RSVD_VIDSTRB_1 O T0409 TPC28T
		RSVD_VIDSTRB1	H8 CPU_RSVD_VIDSTRB_2 O T0410 TPC28T
		RSVD_VIDSTRB2	H9 CPU_RSVD_VIDSTRB_3 O T0411 TPC28T
		RSVD_VIDSTRB3	
		RSVD_VIDSTRB4	
		RSVD_VIDSTRB5	
		RSVD_VIDSTRB6	
		RSVD_VIDSTRB7	
		RSVD_VIDSTRB8	
		RSVD_VIDSTRB9	
		RSVD_VIDSTRB10	
		RSVD_VIDSTRB11	
		RSVD_VIDSTRB12	
		RSVD_VIDSTRB13	
		RSVD_VIDSTRB14	
		RSVD_VIDSTRB15	
		RSVD_VIDSTRB16	
		RSVD_VIDSTRB17	
		RSVD_VIDSTRB18	
		RSVD_VIDSTRB19	
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		RSVD_VIDSTRB43	
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		RSVD_VIDSTRB94	
		RSVD_VIDSTRB95	
		RSVD_VIDSTRB96	
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		RSVD_VIDSTRB98	
		RSVD_VIDSTRB99	
		RSVD_VIDSTRB100	

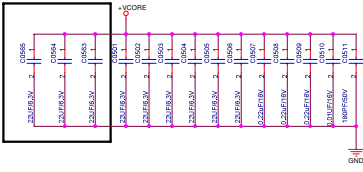
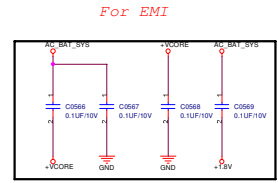
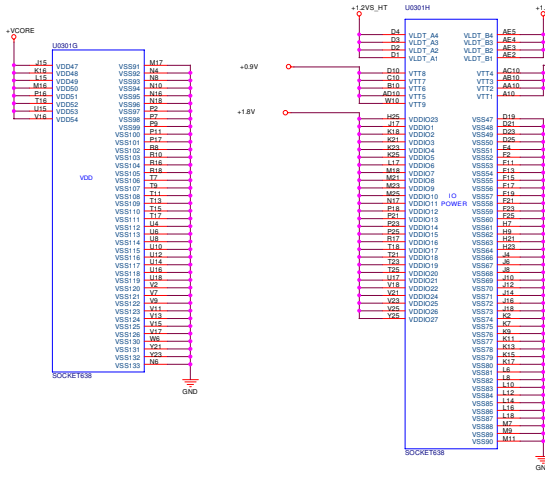
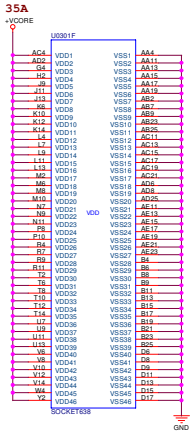


PLEASE CLOSE TO PROCESSOR WITHIN 1.2 INCH

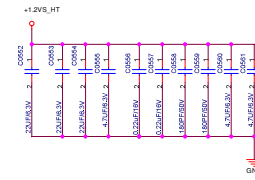
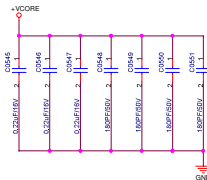
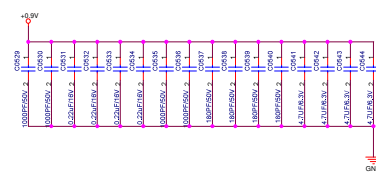
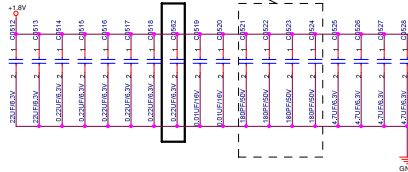
PLEASE CLOSE TO PROCESSOR WITHIN 1.2 INCH

<< Kennedy_Zhang >>


ASUS		Title: FSU	
ASUSTek Computer INC		Engineer: He Wang	
B524	Project Name	Rev	1.0
C	FSU		
Date: 2008-10-20 20:07	Sheet: 4	of	4



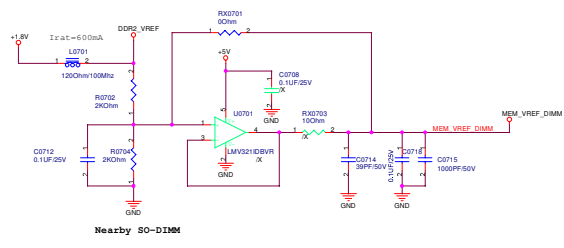
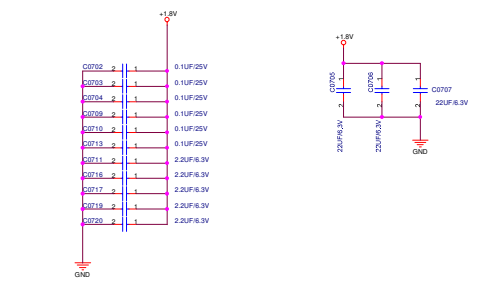
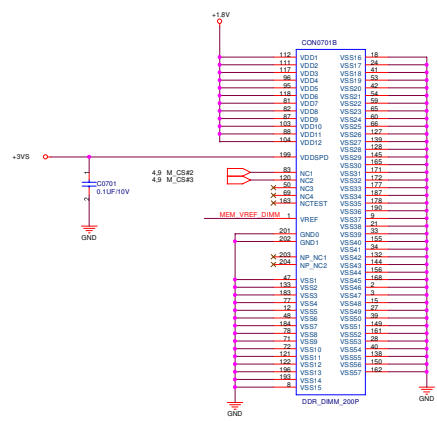
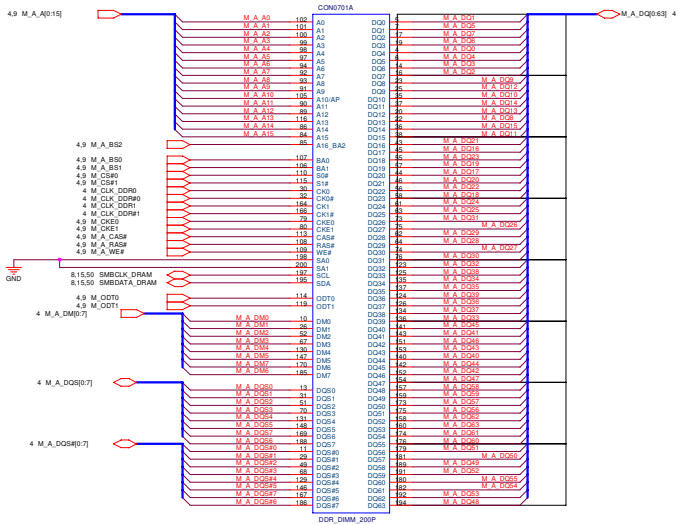
For DDR2 add/cmd refer to split plane.



<< Kennedy_Zhang >>

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-03-29 10:07	Sheet: 6	of	26

« Kennedy_Zhang »



<< Kennedy_Zhang >>

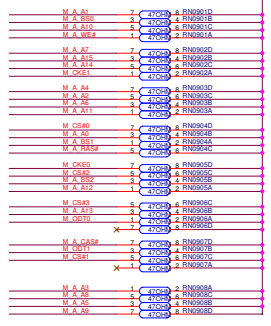
4.7 M_A_A0[15]
4.7 M_A_B0[2]

4.7 M_CS#0
4.7 M_CS#1
4.7 M_CS#2
4.7 M_CS#3

4.7 M_A_WE#
4.7 M_A_CAS#
4.7 M_A_RAS#

4.7 M_CKE0
4.7 M_CKE1

4.7 M_ODT0
4.7 M_ODT1



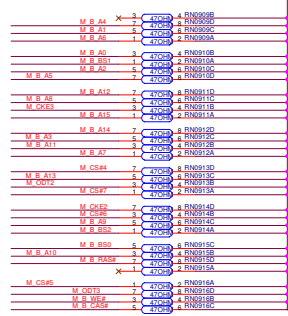
4.8 M_B_A0[15]
4.8 M_B_B0[2]

4.8 M_CS#4
4.8 M_CS#5
4.8 M_CS#6
4.8 M_CS#7

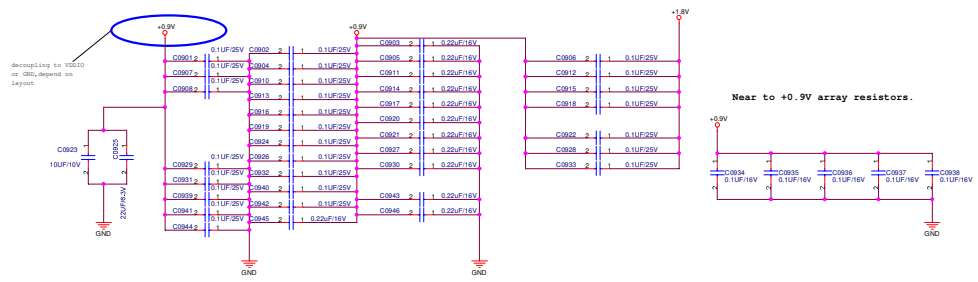
4.8 M_B_WE#
4.8 M_B_CAS#
4.8 M_B_RAS#

4.8 M_CKE2
4.8 M_CKE3

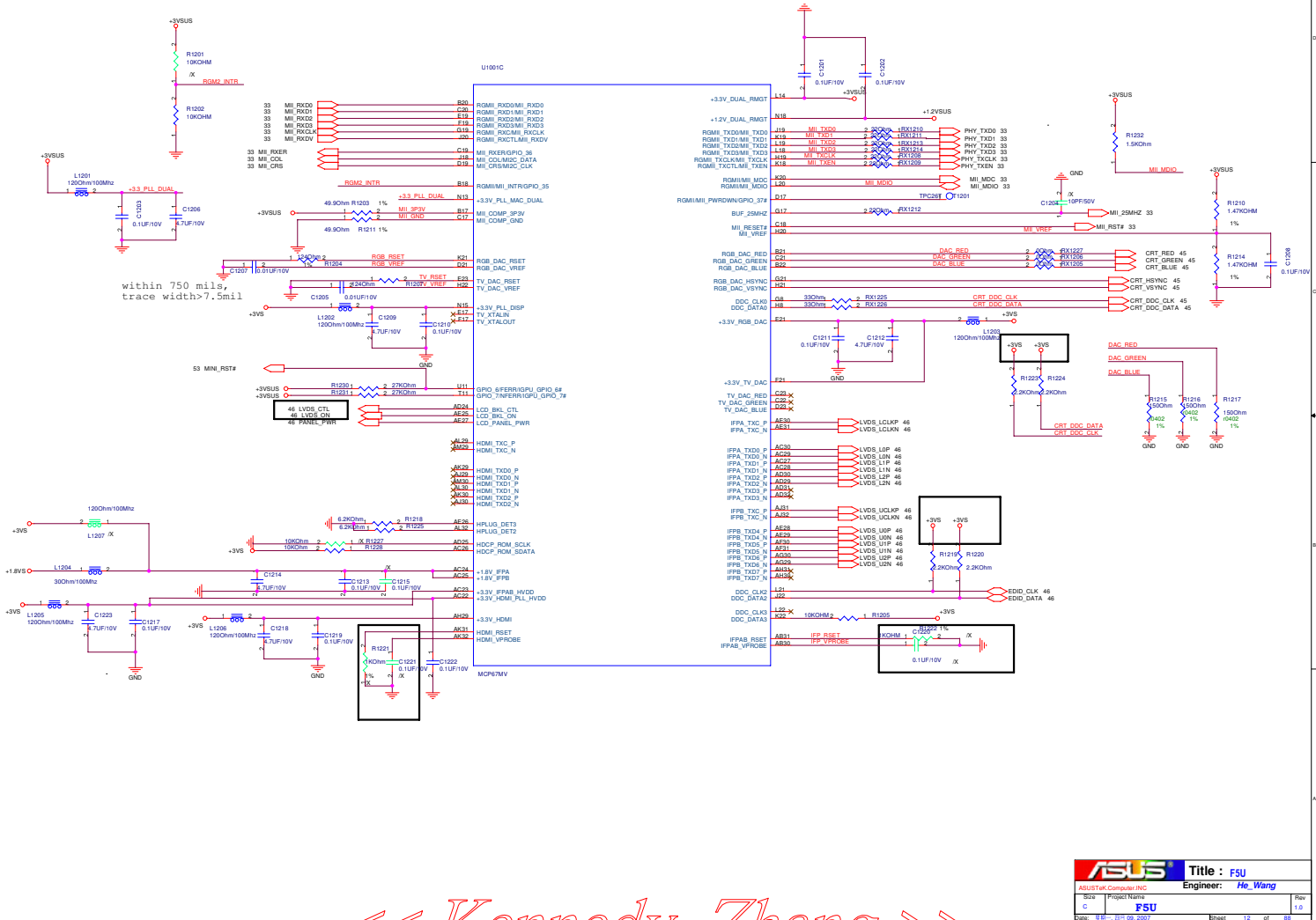
4.8 M_ODT2
4.8 M_ODT3



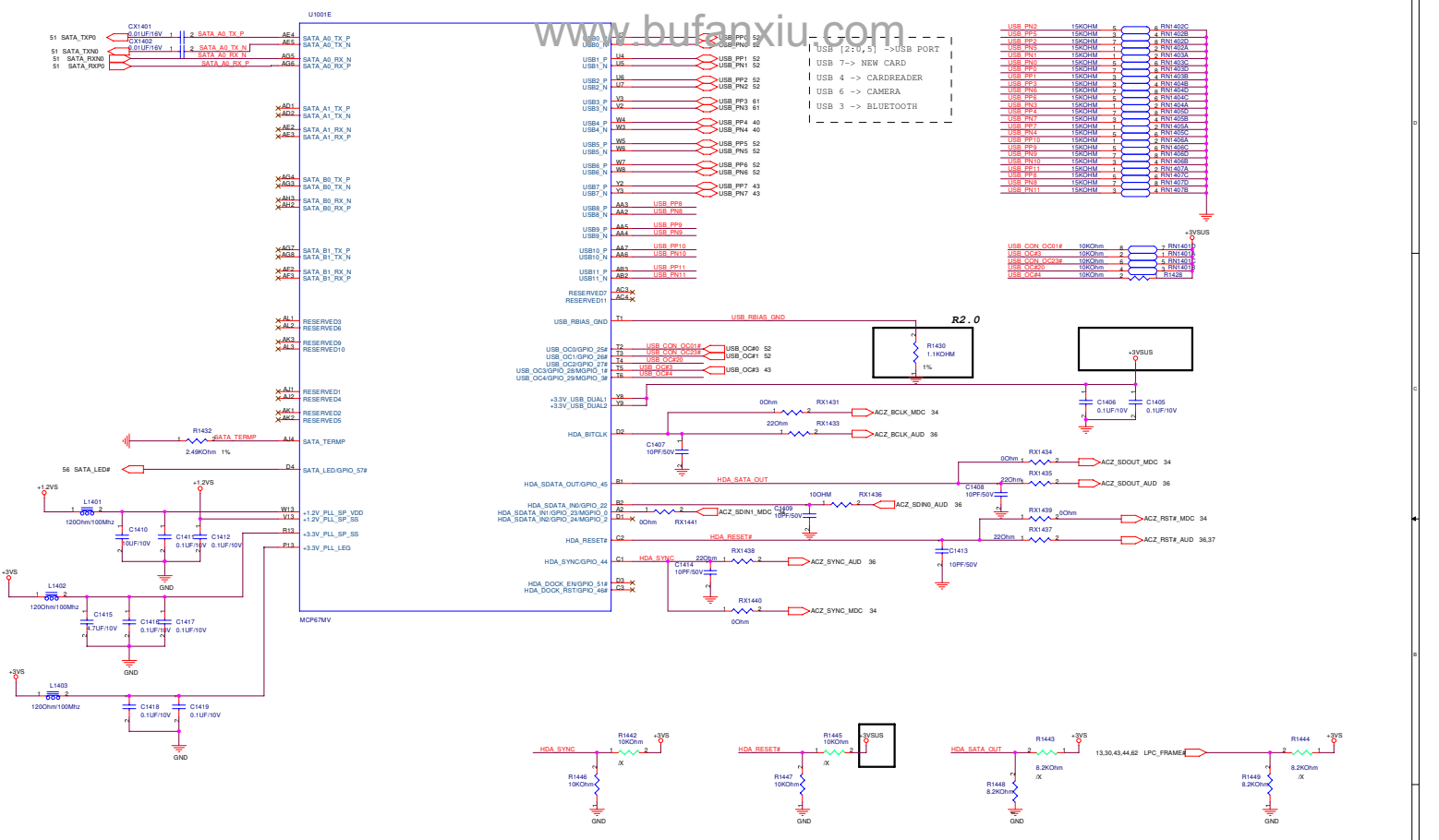
Layout Note: Place one cap close to every 2 pullup resistors terminated to +0.9V



<< Kennedy_Zhang >>



« Kennedy_Zhang »



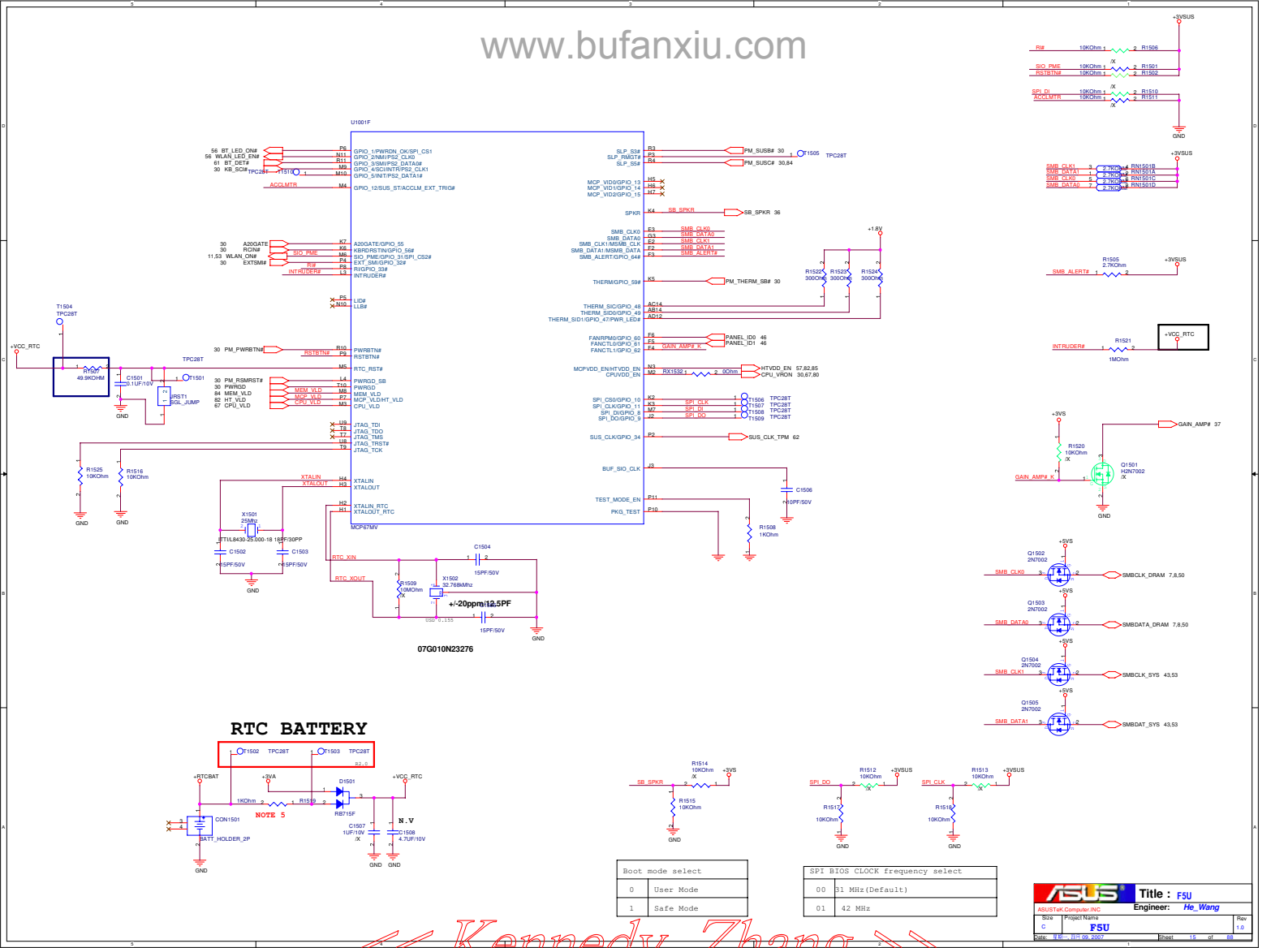
SIO CLOCK select	
0	14.31818 MHz (Default)
1	24 MHz

Networking select	
0	MIII
1	RGMII

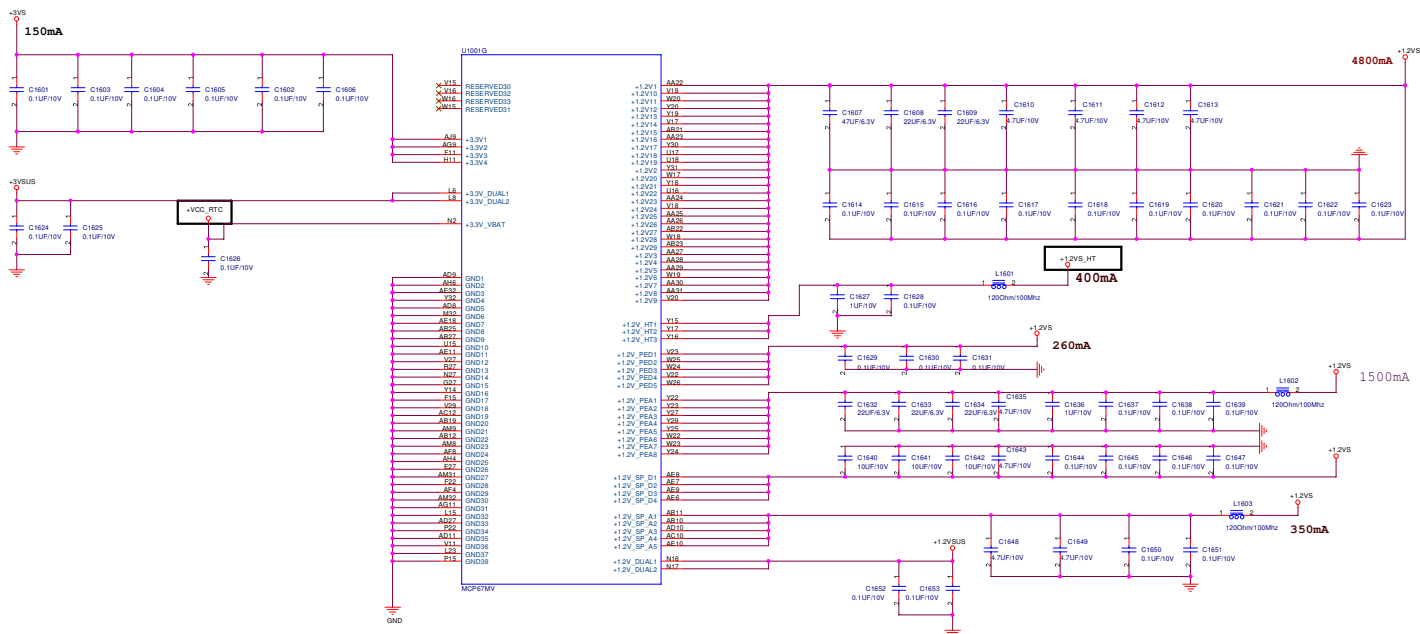
BIOS Select	
00	LPC BIOS
01	PCI BIOS

ASUS Title : FSU
 ASUSTeK Computer INC. Engineer: He Wang
 Rev: C Project Name: FSU Rev: 1.0
 Date: 2016-09-29 20:07 Sheet: 44 of 88

« Kennedy_Zhang »




<< Kennedy_Zhang >>




« Kennedy_Zhang »


ASUS		Title : FSU	
ASUSTek Consumer INC		Engineer: He Wang	
B528	Project Name		Rev
C	FSU		1.0
Date: 2010-05-20 10:00		Sheet: 16	of 20

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-01-26 10:07		Sheet: 18	of 28


« Kennedy_Zhang »

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU		1.0
Date: 2011-01-26 10:07	Sheet: 18	of	28


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 25	of 28


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 21	of 28


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 25	of 28


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 21	of 28


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 24	of 28


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 25	of 28


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 25	of 25


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 21	of 28

« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 25	of 25

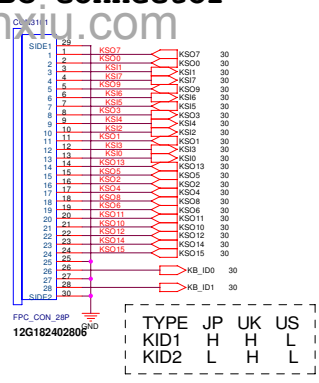
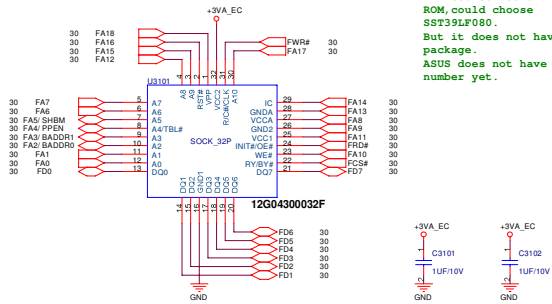
« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 25	of 25

« Kennedy_Zhang »

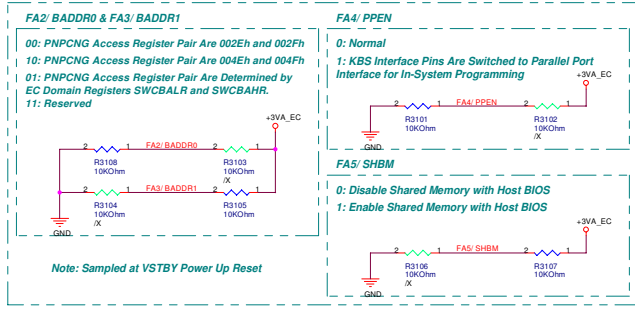
ISA ROM (4Mbits)

SST-PLCC32 4Mbits Flash ROM
PN:05G001014110
(FLASH SST S39VF040-70-4C-NHE
4M-70 PLCC-32)
If need to use 8Mbits ISA
ROM, could choose
SST39LF080.
But it does not have PLCC32
package.
ASUS does not have part
number yet.




ISA ROM

EC Hardware Strapping

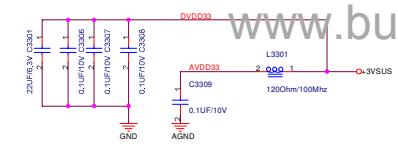


ASUS Title: FSU
ASUS Tek Computer INC Engineer: He_Wang
Size Custom Project Name FSU Rev 1.0
Date: 11/11/2007 Sheet 31 of 38

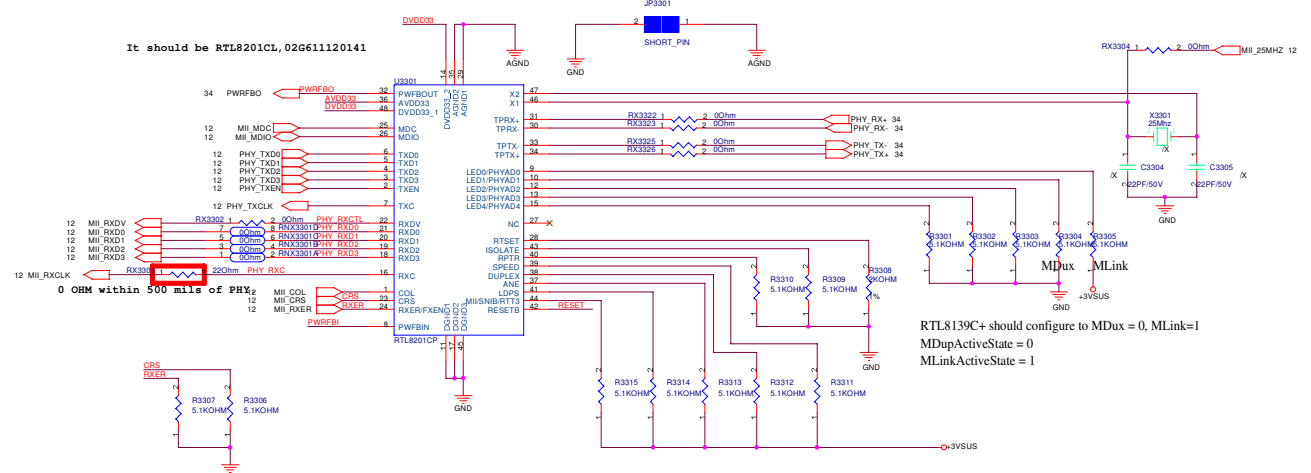
<< Kennedy_Zhang >>

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-01-26 10:07	Sheet: 01	of	01

« Kennedy_Zhang »

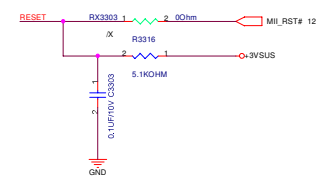
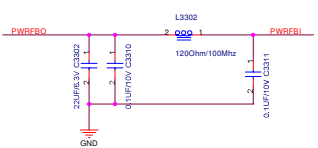


It should be RTL8201CL, 02G61120141



RTL8139C+ should configure to MDux = 0, MLink = 1
 MDupActiveState = 0
 MLinkActiveState = 1

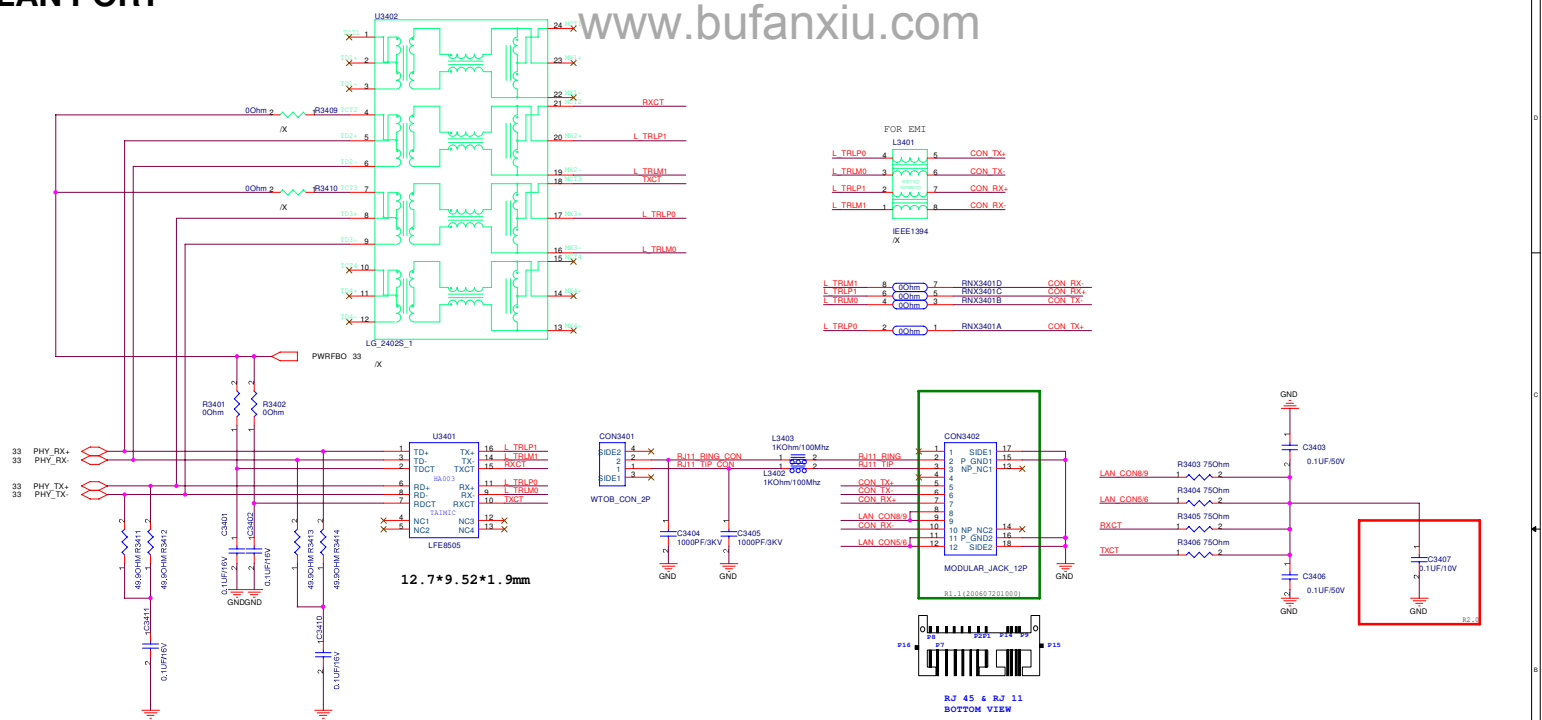
- ISOLATE:** set high to isolate the RTL8201CP from the MAC. this will also isolate the MC/MDIO management interface
- RPTR:** set high to put the RTL8201CP into repeater mode
- SPEED:** this pin is latched to input during a power on or reset condition. set high to put the RTL8201CP into 100Mbps operation
- DUPLEX:** Set high to enable full duplex
- ANE:** Set high to enable auto-negotiation mode, set low to force mode
- LDPS:** set high to put the RTL8201CP into LDPS mode
- MII/SNIB:** pull high to set the RTL8201CP into MII mode operation. set low for SMI mode



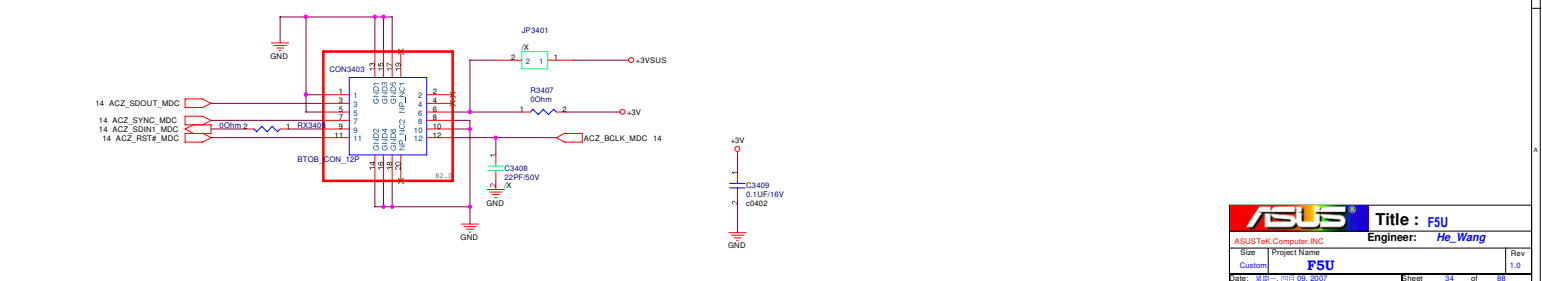
ASUS		Title : FSU	
ASUSTek Computer, INC		Engineer: He_Wang	
Size	Project Name	Rev	
Custom	FSU	1.0	
Date: 2011.09.20	Sheet: 33	of	38

<< Kennedy_Zhang >>

LAN PORT



MDC CONN.



ASUS		Title : FSU	
ASUSTek Computer, INC	Project Name	Engineer: He_Wang	Rev
Custom	FSU		1.0
Date: 2011.09.20	Drawn: 34	of	38

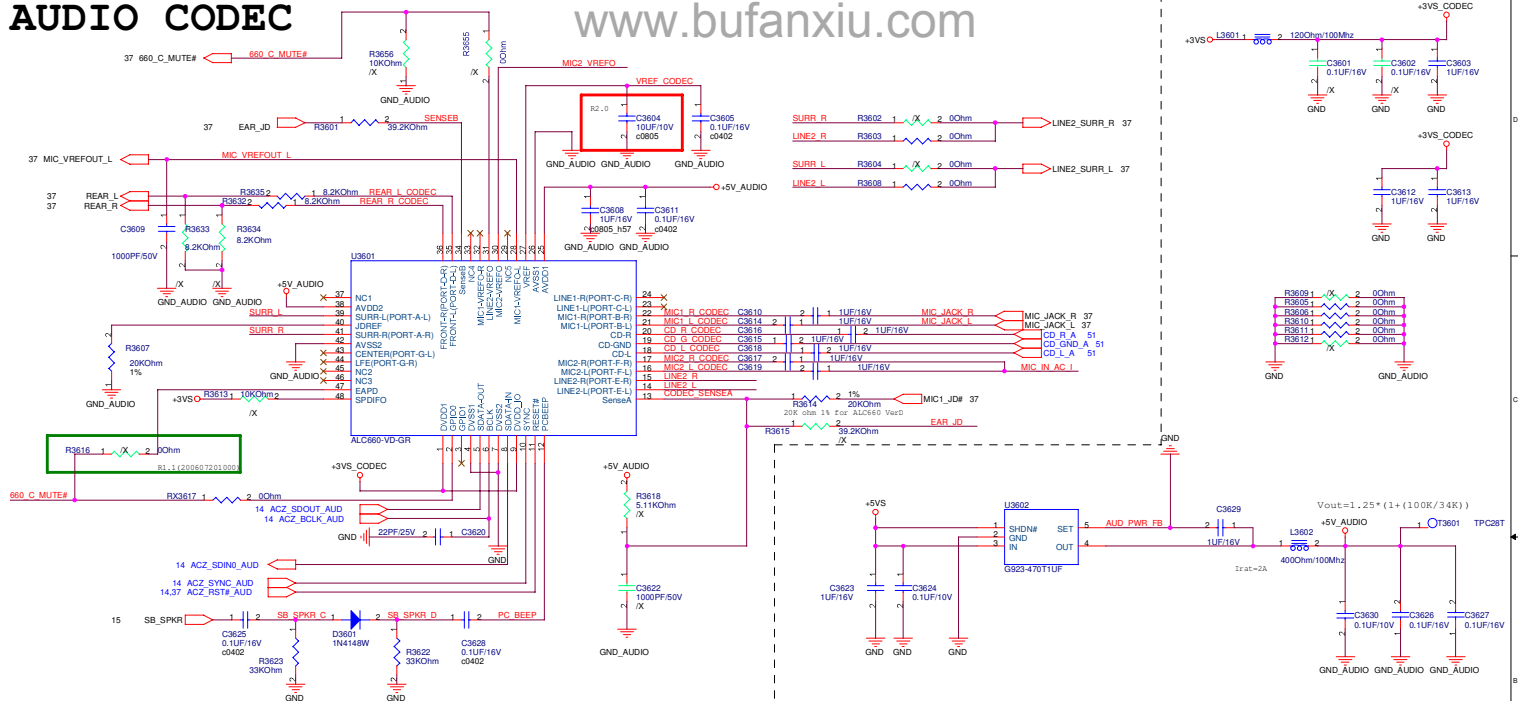
<< Kennedy_Zhang >>

		Title : FSU	
ASUSTek Computer INC		Engineer: He_Wang	
Size	Project Name		Rev
Custom	FSU		1.0
Date: 2011-11-28 20:07		Sheet	35 of 38

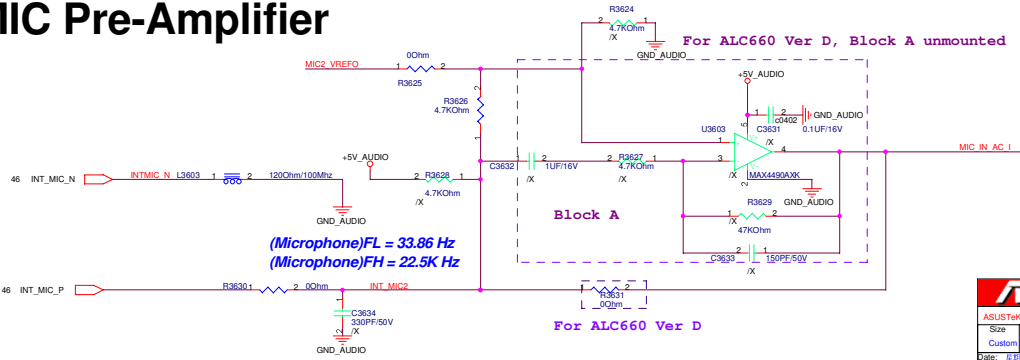
<< Kennedy_Zhang >>

AUDIO CODEC

www.bufanxiu.com



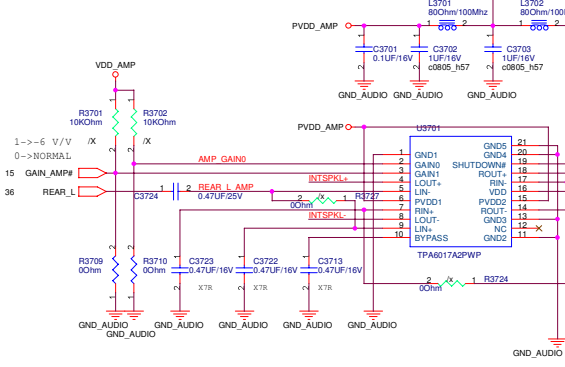
Internal MIC Pre-Amplifier



ASUS		Title : FSU	
ASUSTek Computer, Inc		Engineer: He_Wang	
Size	Project Name	Date	Rev
Custom	FSU	11/11/09	1.0
Date: 11/11/09		Sheet	36 of 38

<< Kennedy_Zhang >>

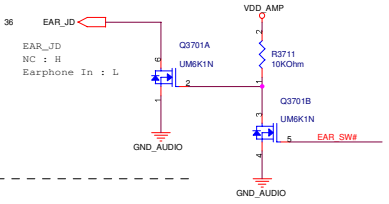
AUDIO AMPLIFIER



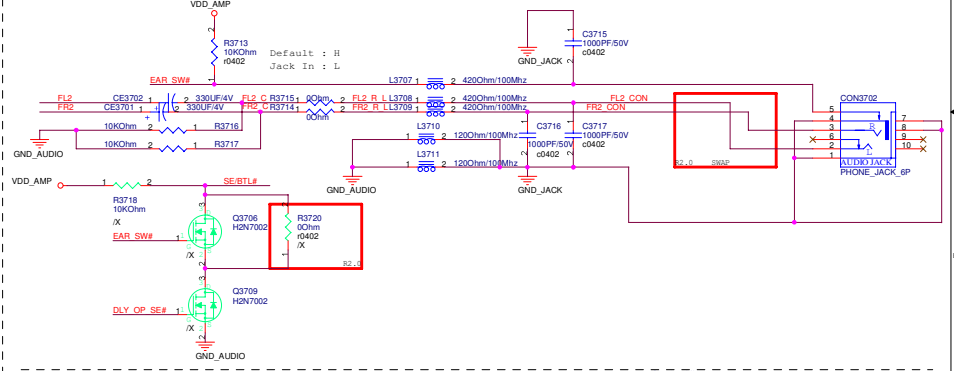
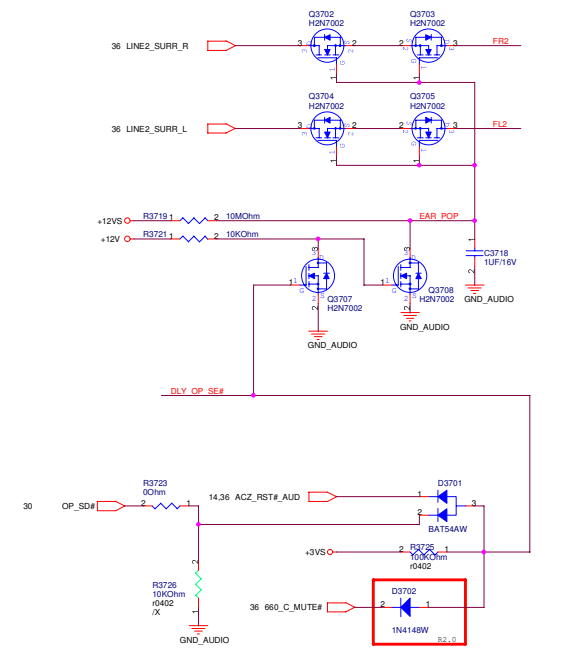
SPEAKER



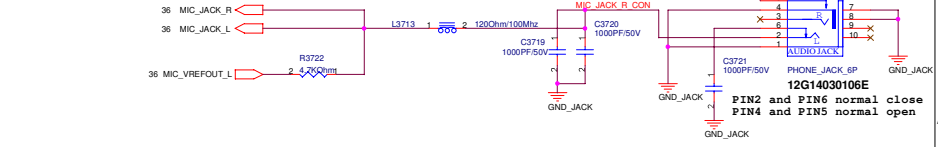
HeadPhone



DEPOP CIRCUIT



External Microphone




ASUS		Title : FSU
ASUSTek Computer, INC	Project Name	Engineer: He_Wang
Size	Custom	FSU
Date: 11/15/08	11/15/08	37 of 88

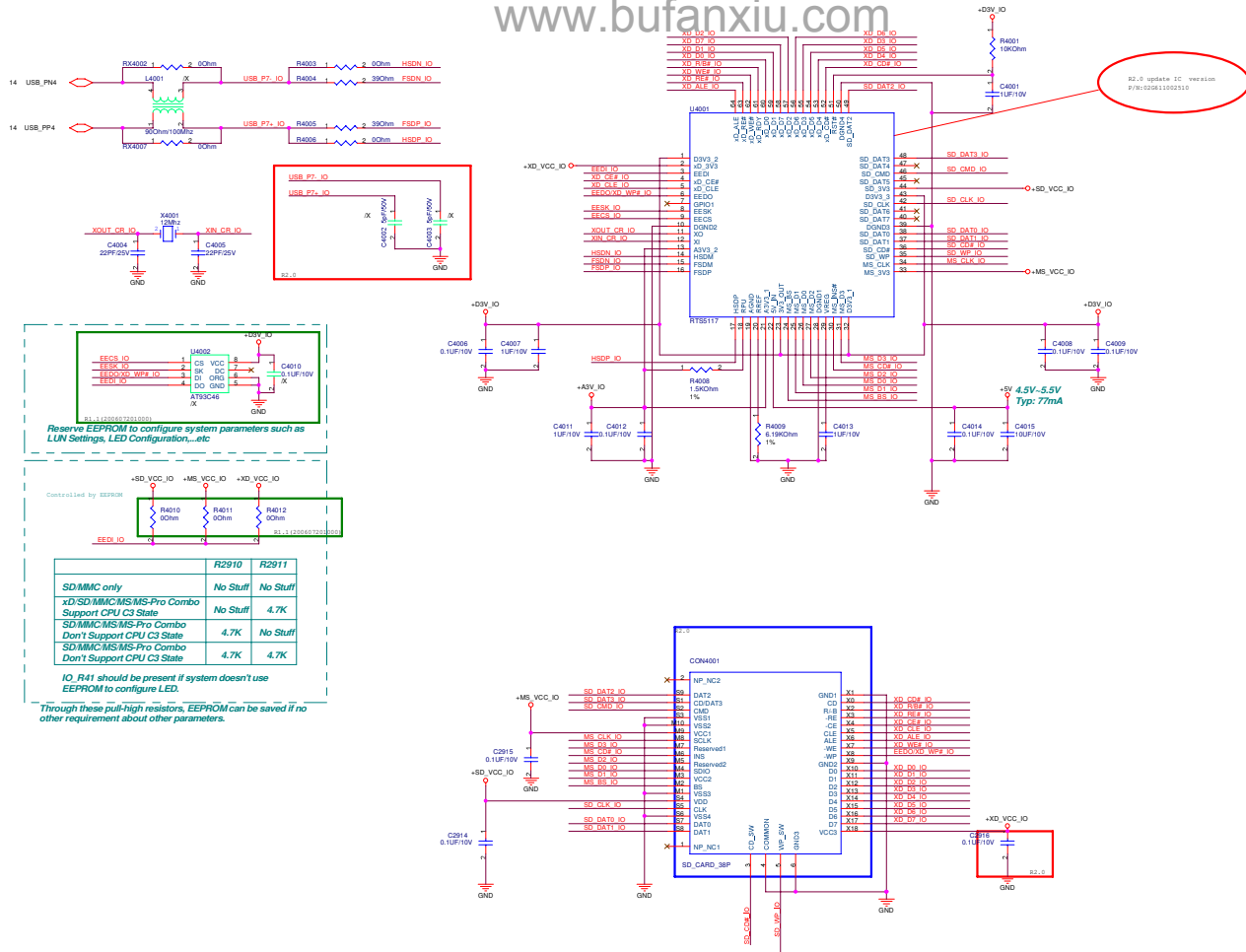
<< Kennedy_Zhang >>

		Title : FSU	
ASUSTeK Computer INC		Engineer: He_Wang	
Size	Project Name		Rev
Custom	FSU		1.0
Date: 2007-11-28		Sheet	38 of 38

<< Kennedy_Zhang >>

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-01-26 10:07	Sheet: 01	of	01

« Kennedy_Zhang »



Reserve EEPROM to configure system parameters such as LUN Settings, LED Configuration...etc




	R2910	R2911
SD/MMC only	No Stuff	No Stuff
xD/SD/MMC/MS/MS-Pro Combo Support CPU C3 State	No Stuff	4.7K
SD/MMC/MS/MS-Pro Combo Don't Support CPU C3 State	4.7K	No Stuff
SD/MMC/MS/MS-Pro Combo Don't Support CPU C3 State	4.7K	4.7K


IO_R41 should be present if system doesn't use EEPROM to configure LED.

Through these pull-high resistors, EEPROM can be saved if no other requirement about other parameters.

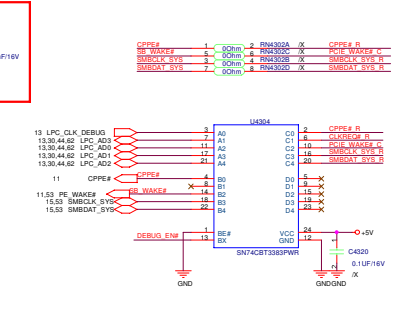
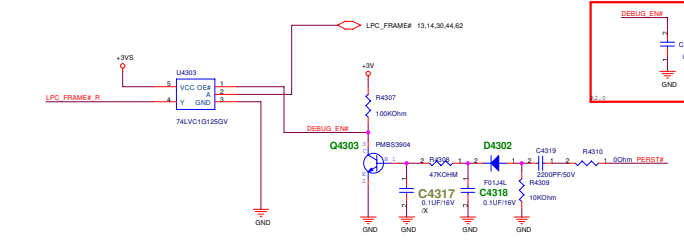
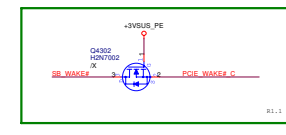
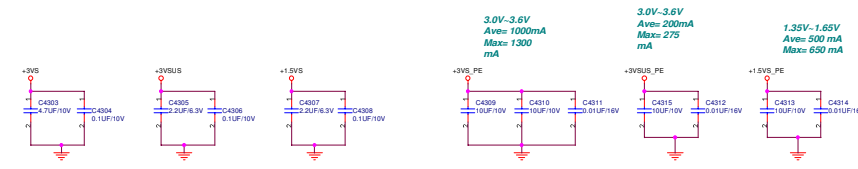
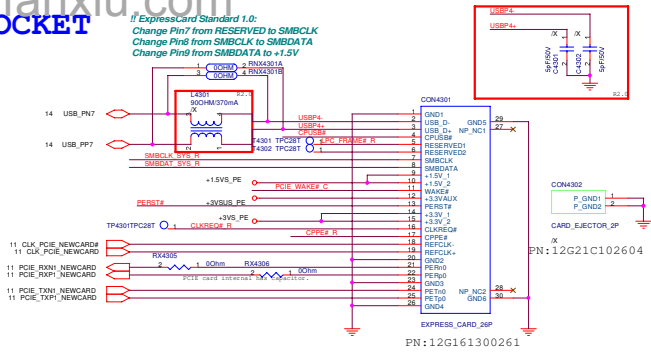
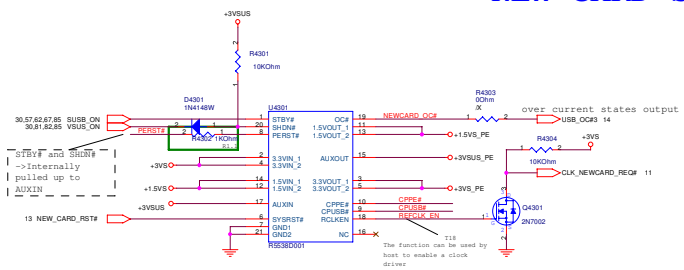
<< Kennedy_Zhang >>

		Title : FSU
ASUSTeK Computer INC		Engineer: He_Wang
Size	Project Name	Rev
Custom	FSU	1.0
Date: 11/23/2007	Sheet	41 of 88

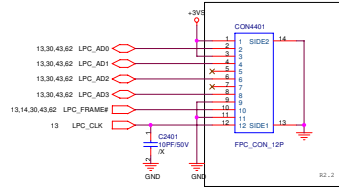
<< Kennedy_Zhang >>

		Title : F5U	
ASUSTeK Computer INC.		Engineer: He Wang	
Size	Project Name		Rev
Custom	F5U		1.0
Date: 11/28/2007		Sheet 42 of 69	

<< *Kennedy_Zhang* >>

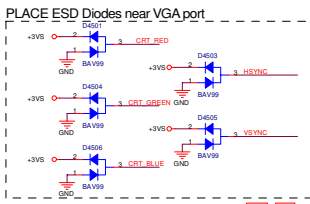
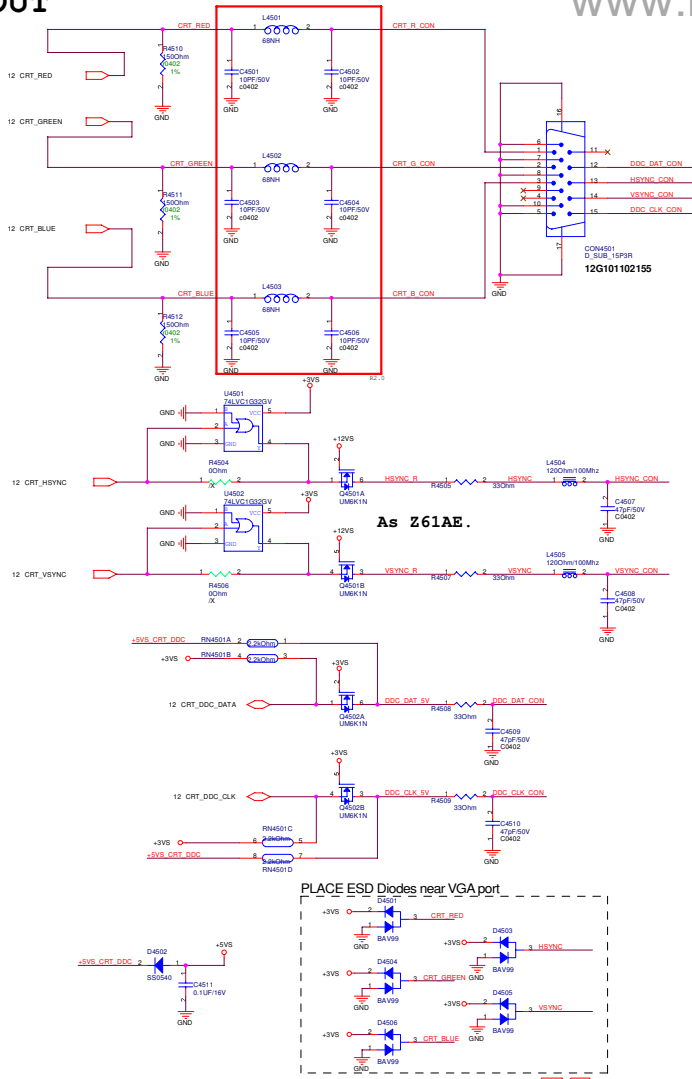


« Kennedy_Zhang »



« Kennedy_Zhang »

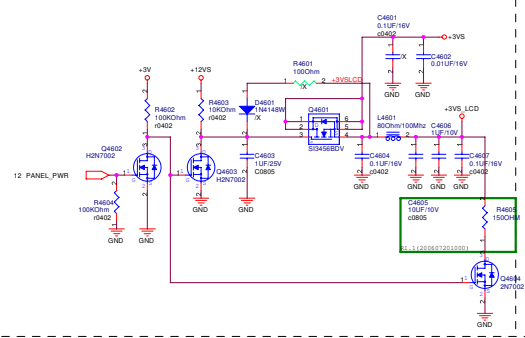
		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-01-26 10:07	Sheet: 44	of	88



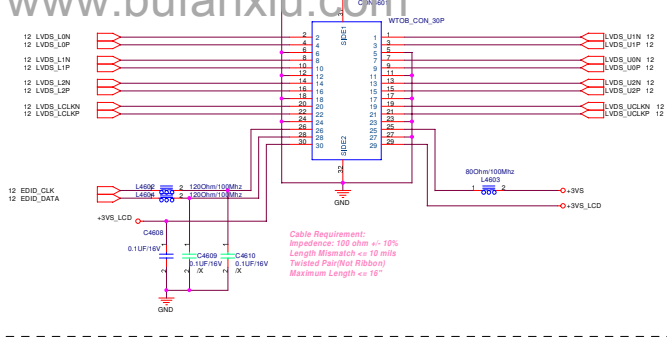
« Kennedy_Zhang »

ASUS		Title : FSU	
ASUSTek Computer INC		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-07-29 10:07	Sheet: 45	of	48

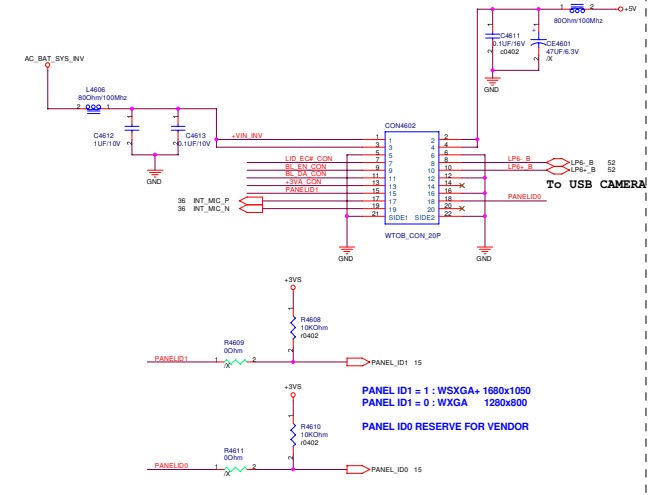
LCD Power



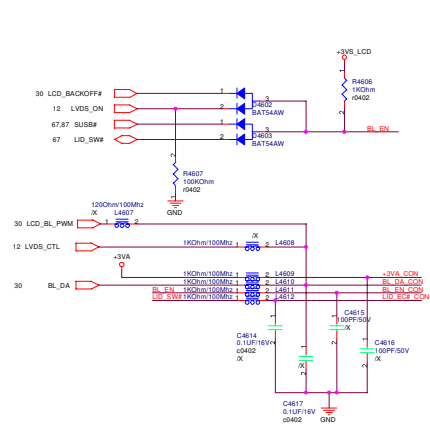
LCD LVDS Interface




INVERTER Interface




Backlight Enable




« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC		Engineer: He_Wang	
Size	Project Name		Rev
Custom	FSU		1.0
Date: 2007-11-28		Sheet	47 of 88

<< Kennedy_Zhang >>

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-01-26 10:07	Sheet: 48	of	50

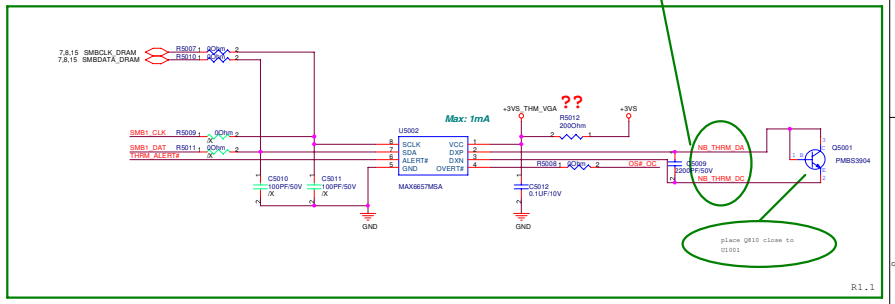
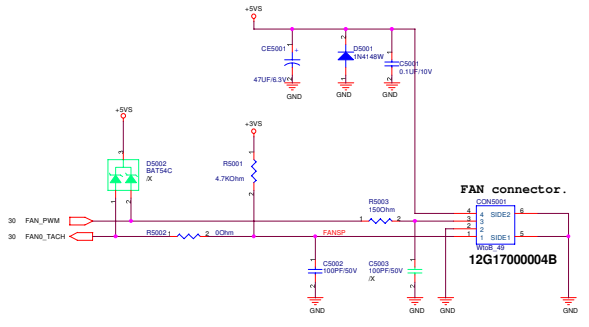
« Kennedy_Zhang »

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-05-26 10:07		Sheet: 41	of 48

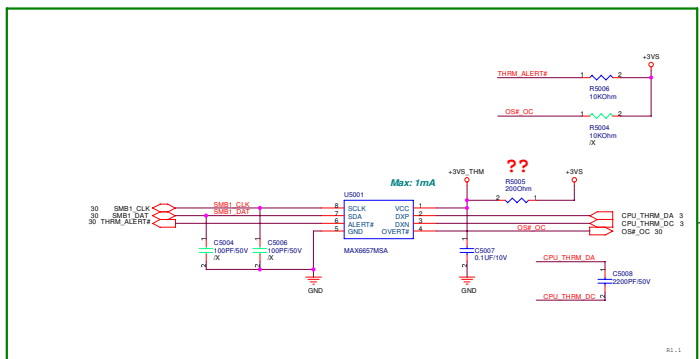
« Kennedy_Zhang »

DC FAN control

-----OTHER SIGNALS
 15 mils
 -----GND
 10 mils
 -----NB_THRM_DA(10 mils)
 10 mils
 -----NB_THRM_DC(10 mils)
 10 mils
 -----GND
 15 mils
 -----OTHER SIGNALS
 Avoid FSB,Power



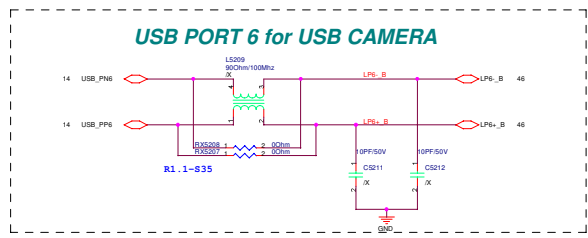
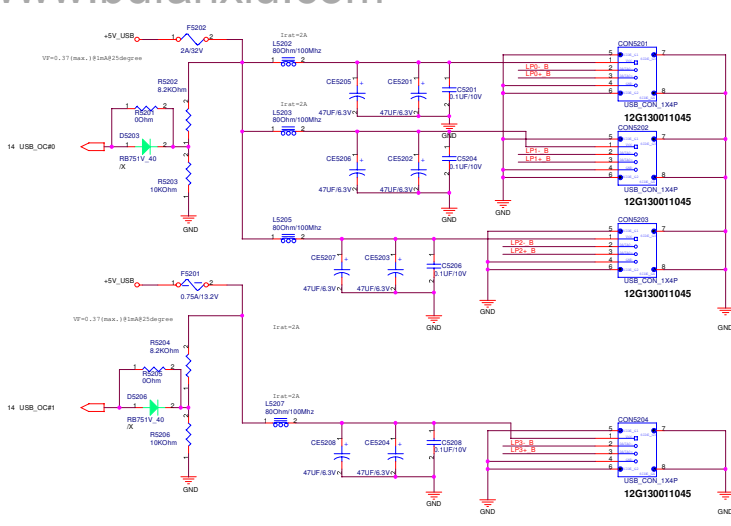
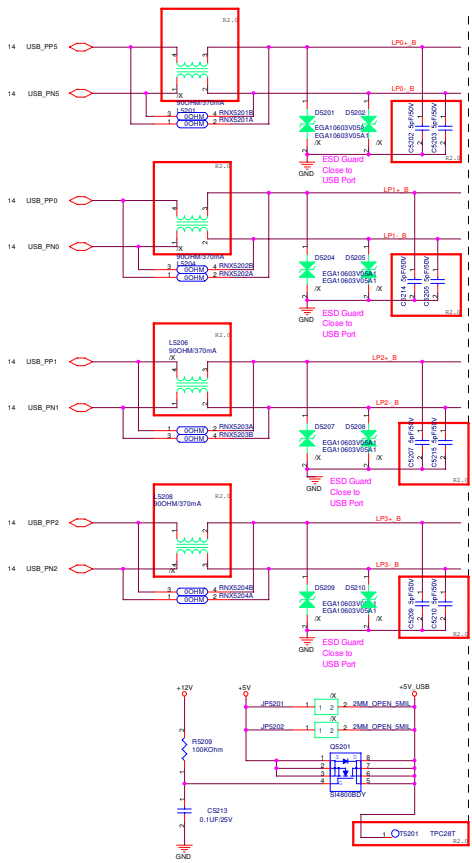
Thermal Sensor



Route CPU_THRM_DA and CPU_THRM_DC on the same layer
 15 mils
 -----GND
 10 mils
 -----H_THERMDA(10 mils)
 10 mils
 -----H_THERMDC(10 mils)
 10 mils
 -----GND
 15 mils
 -----OTHER SIGNALS
 Avoid FSB,Power

ASUS		Title : FSU	
ASUSTek Computer INC		Engineer: He_Wang	
Size	Project Name	Rev	
C	FSU	1.0	
DATE: 8/8	10/28/2007	Sheet	30 of 38

« Kennedy_Zhang »




« Kennedy_Zhang »

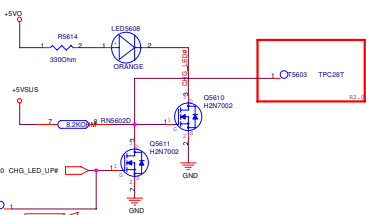
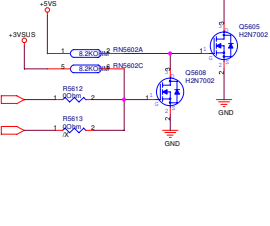
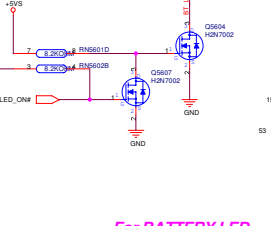
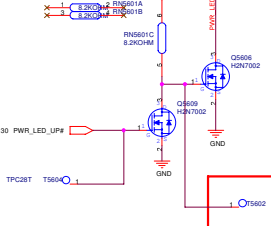
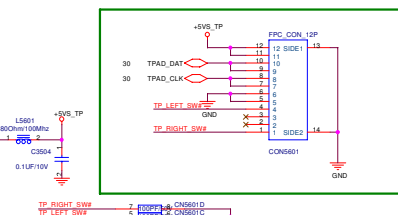
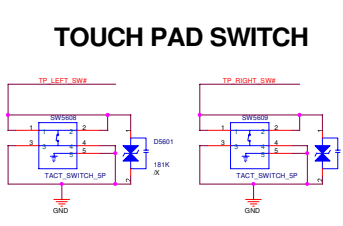
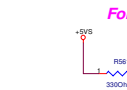
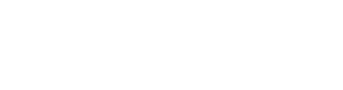
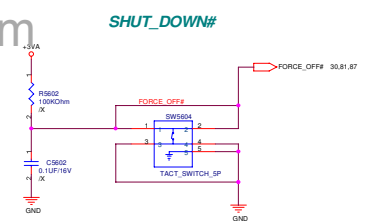
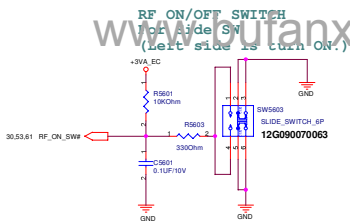
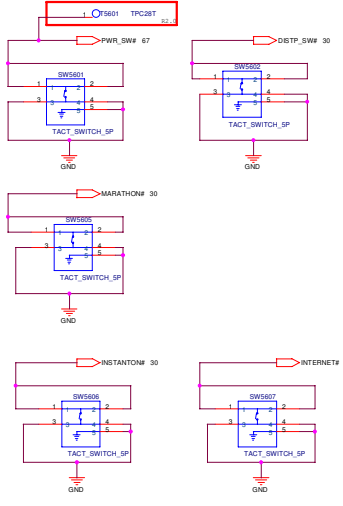
ASUS		Title : FSU	
ASUSTek Computer INC.		Engineer: He Wang	
BSZ	Project Name	Rev	
C	FSU	1.0	
Date: 2011-01-26 13:07	Sheet: 51	of	58

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-01-26 10:07		Sheet: 54	of 58

« Kennedy_Zhang »

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-01-26 10:07		Sheet: 05	of 05

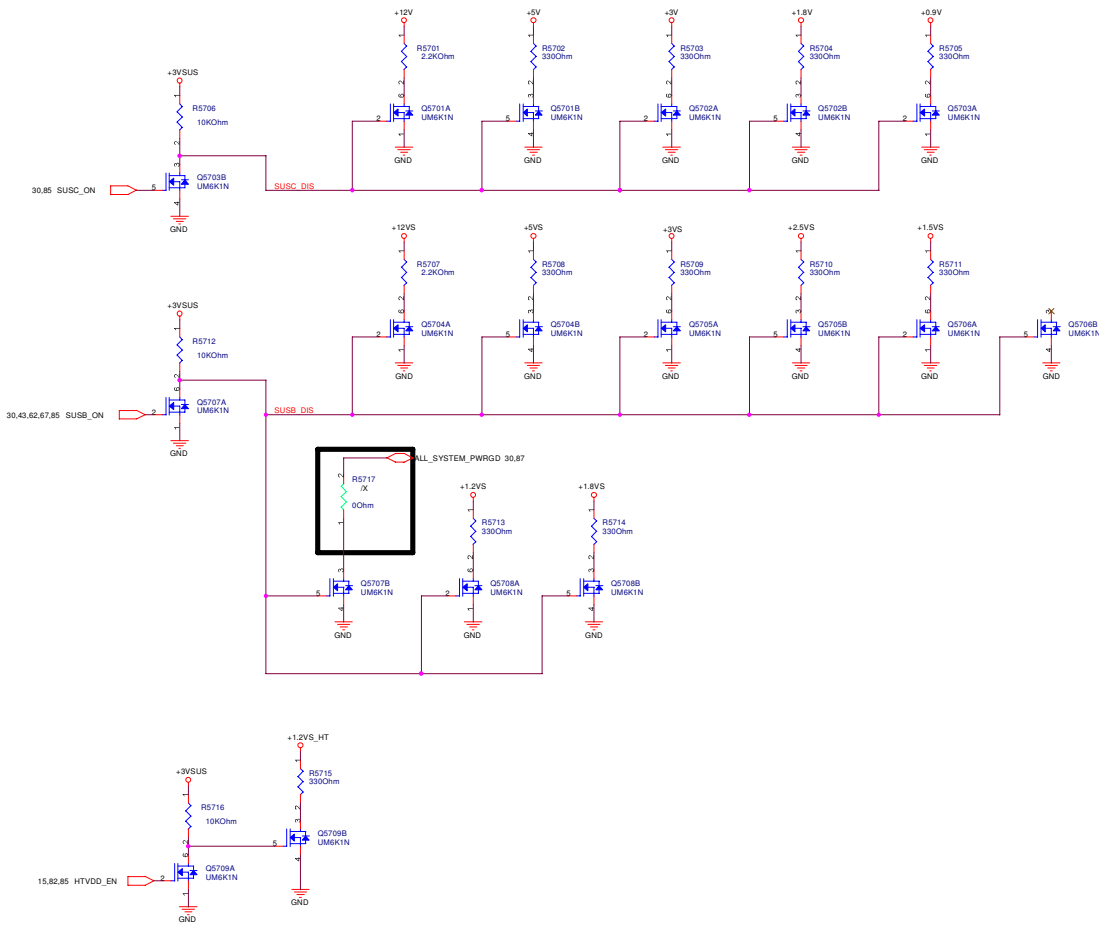
« Kennedy_Zhang »



« Kennedy_Zhang »


ASUS		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Rev	Project Name	Rev	
1	FSU	1.0	
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DISCHARGE CIRCUIT




		Title : FSU	
ASUSTek Computer, INC		Engineer: He_Wang	
Size	Project Name	Rev	
Custom	FSU	1.0	
Date	File Path	Sheet	of
2011.09.20	...	37	38

<< Kennedy_Zhang >>

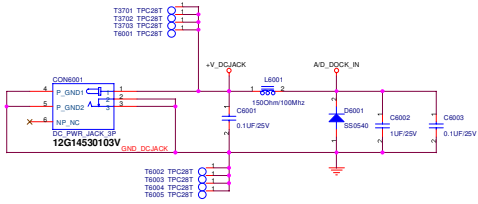
		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-01-26 10:07		Sheet: 01	of 01

« Kennedy_Zhang »

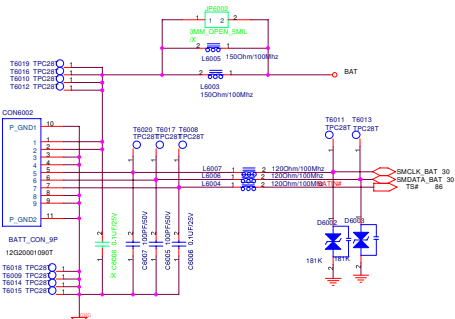
		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU		1.0
Date: 2011-01-26 10:07	Sheet: 01	of	01

« Kennedy_Zhang »

Adaptor IN Circuit



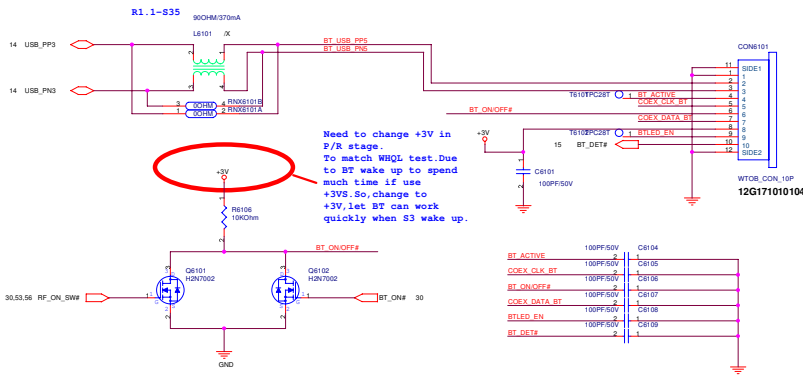
BATTERY IN CIRCUIT



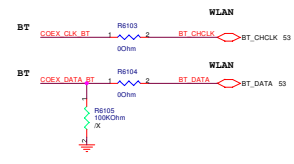
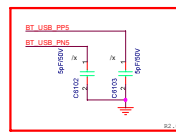
<< Kennedy_Zhang >>

		Title : FSU	
ASUSTek Computer INC		Engineer: He Wang	
Size	Project Name	Rev	1.0
C	FSU		
Date: 2011-01-26 10:07	Sheet: 61	of	68

BLUETOOTH CONNECTOR

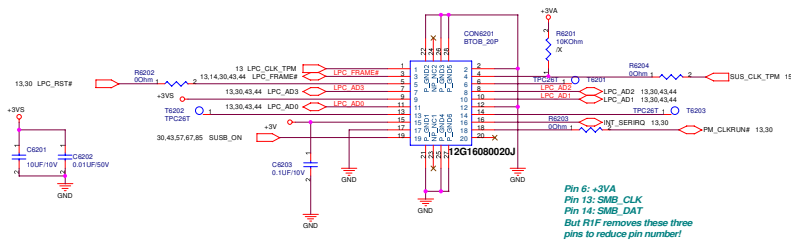


Signal direction-
CLK: BT -> WLAN;
DATA: WLAN -> BT




<< Kennedy_Zhang >>

TPM CONN.




« Kennedy_Zhang »


ASUS		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
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		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
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« Kennedy_Zhang »

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-01-26 10:07		Sheet: 64	of 68

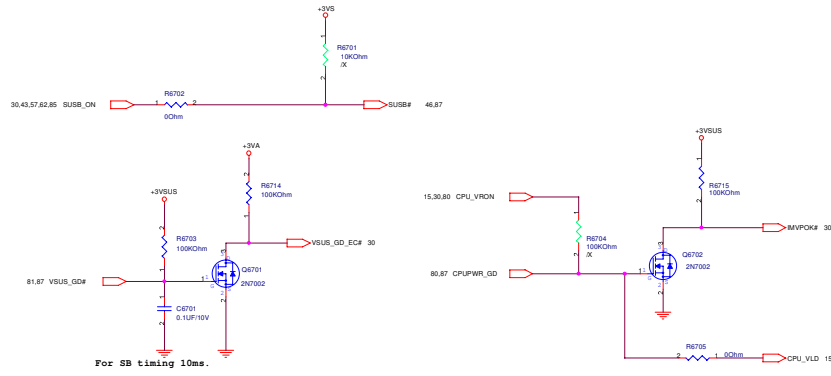
« Kennedy_Zhang »

		Title : FSU	
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Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-05-26 10:07	Sheet: 65	of	66

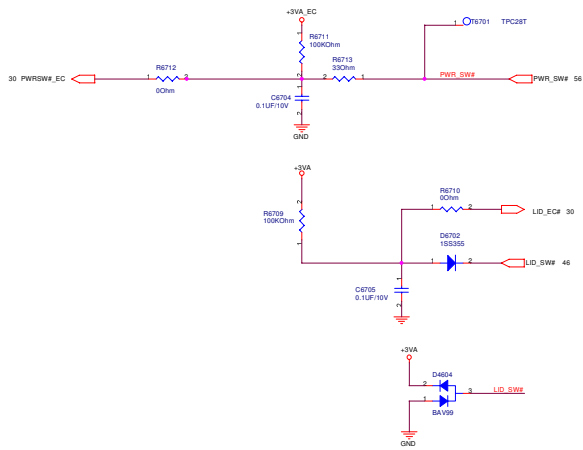
<< Kennedy_Zhang >>

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-01-26 10:07	Sheet: 01	of	01

« Kennedy_Zhang »

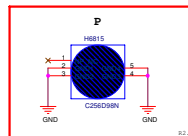
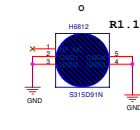
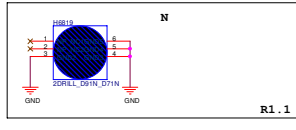
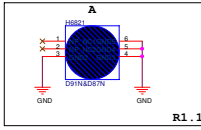
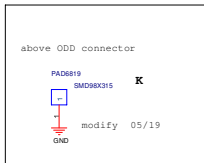
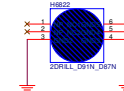
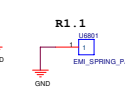
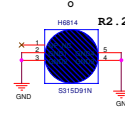
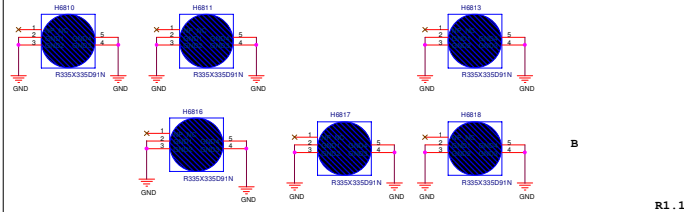
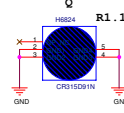
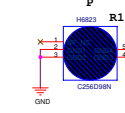
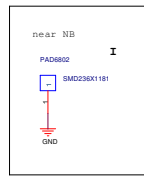
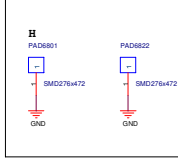
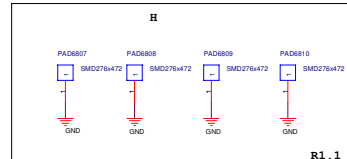
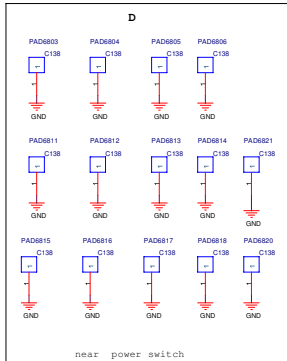
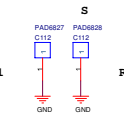
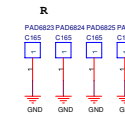
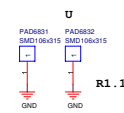
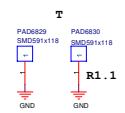
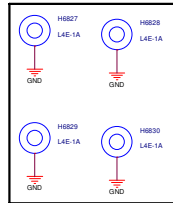
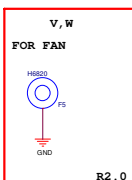
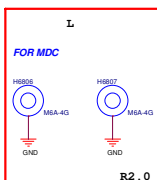
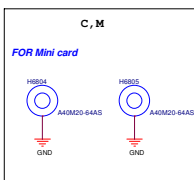
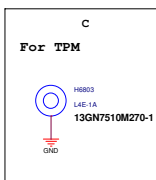
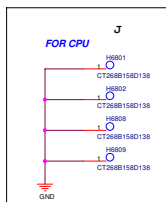


POWER SWITCH




ASUS		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
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<< Kennedy_Zhang >>




H825
C1100150N
H826
C1100150N


« Kennedy_Zhang »

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-01-26 10:07		Sheet: 01	of 01


« Kennedy_Zhang »

		Title : FSU	
ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2011-01-26 10:07		Sheet: 01	of 01


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date:	2014-12-26 20:07	Sheet:	11 of 28


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 15	of 28


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 13	of 28


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 14 of 28	


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 15	of 28


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2017-11-28 20:07		Sheet: 16	of 28


« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2014-12-26 2017		Sheet: 11 of 28	

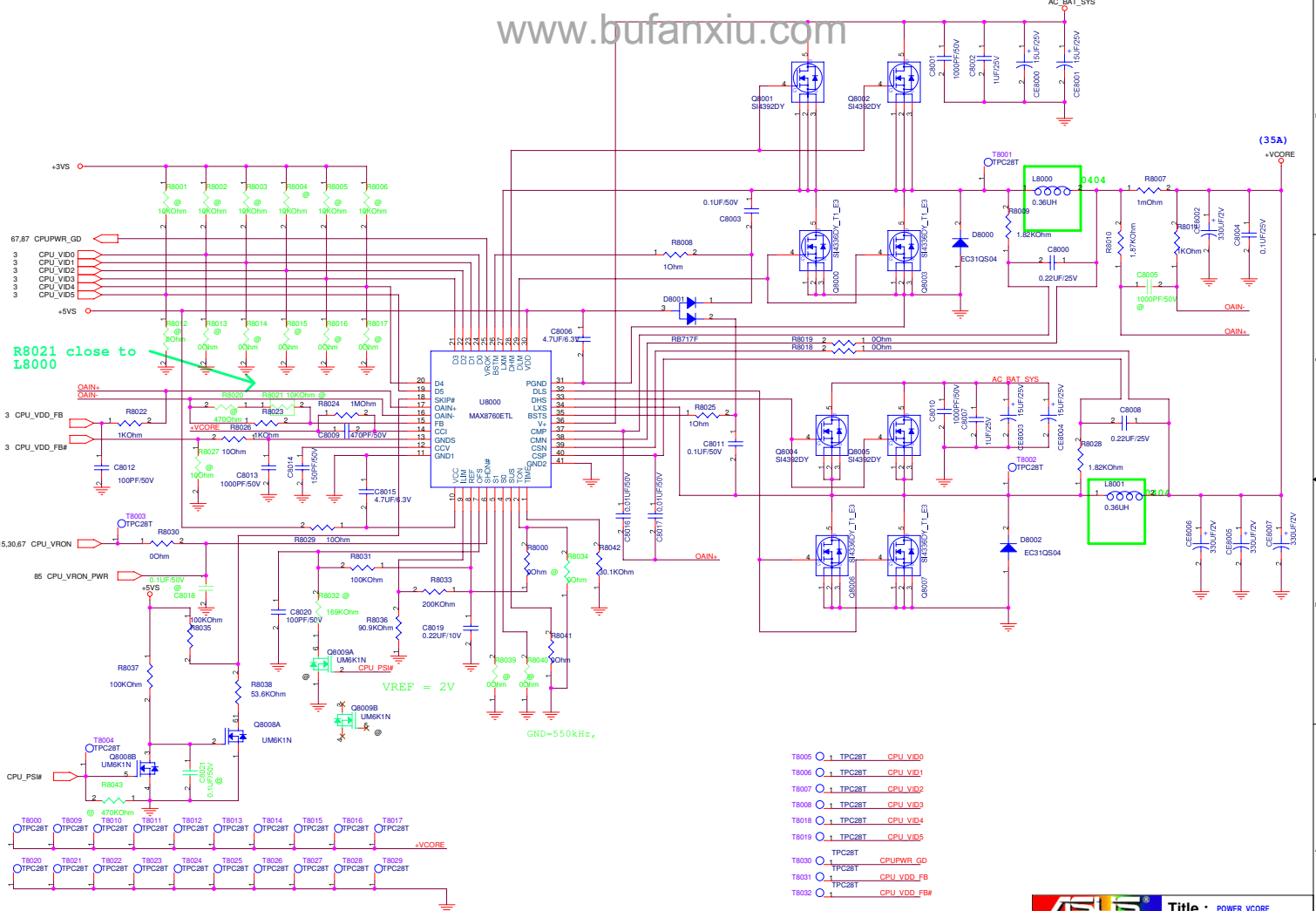
« Kennedy_Zhang »

		Title : FSU	
ASUSTeK Computer INC.		Engineer: He_Wang	
Size	Project Name		Rev
C	FSU		1.0
Date: 2017-11-28 20:07		Sheet: 15	of 25

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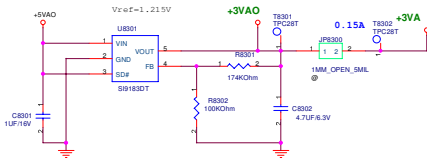
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ASUSTek Computer Inc.		Engineer: He Wang	
Size	Project Name	Rev	
C	FSU	1.0	
Date: 2011-01-26 10:07	Sheet: 01	of	01

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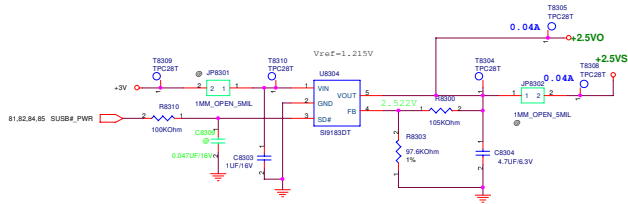


ASUS		Title : POWER_VCORE	
ASUSTek	Project Name	Engineer: li-mei_chen	
Size	Custom	F5N	Rev 1.1
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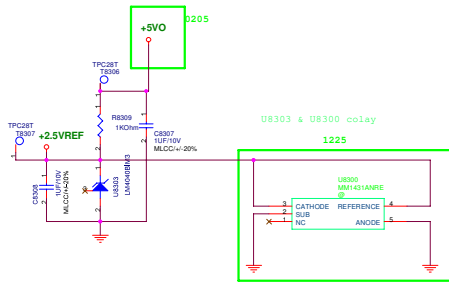
<< Kennedy_Zhang >>



+3VA



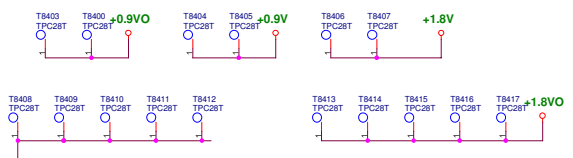
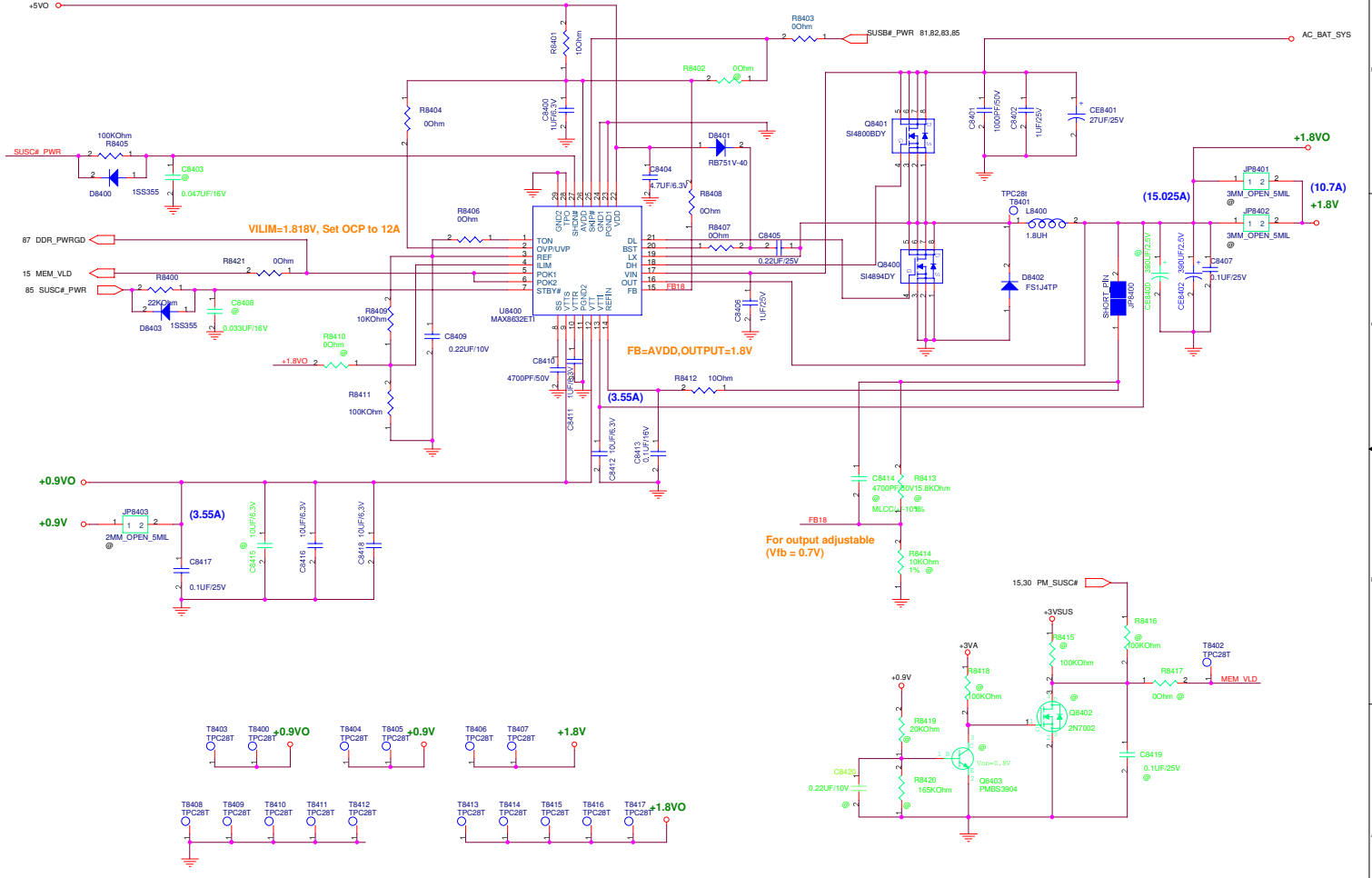
+2.5VS



+2.5VREF

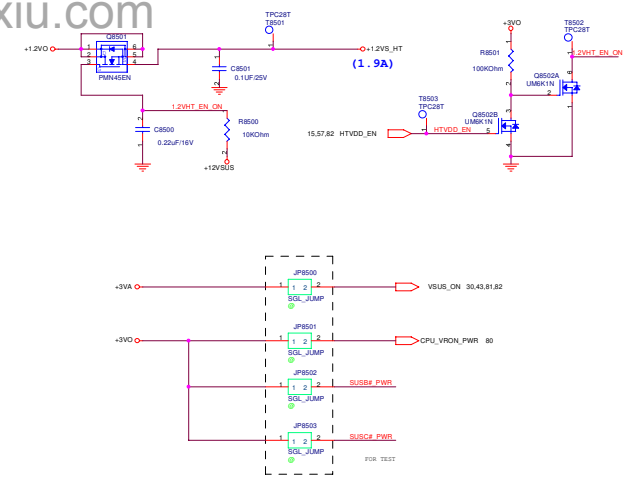
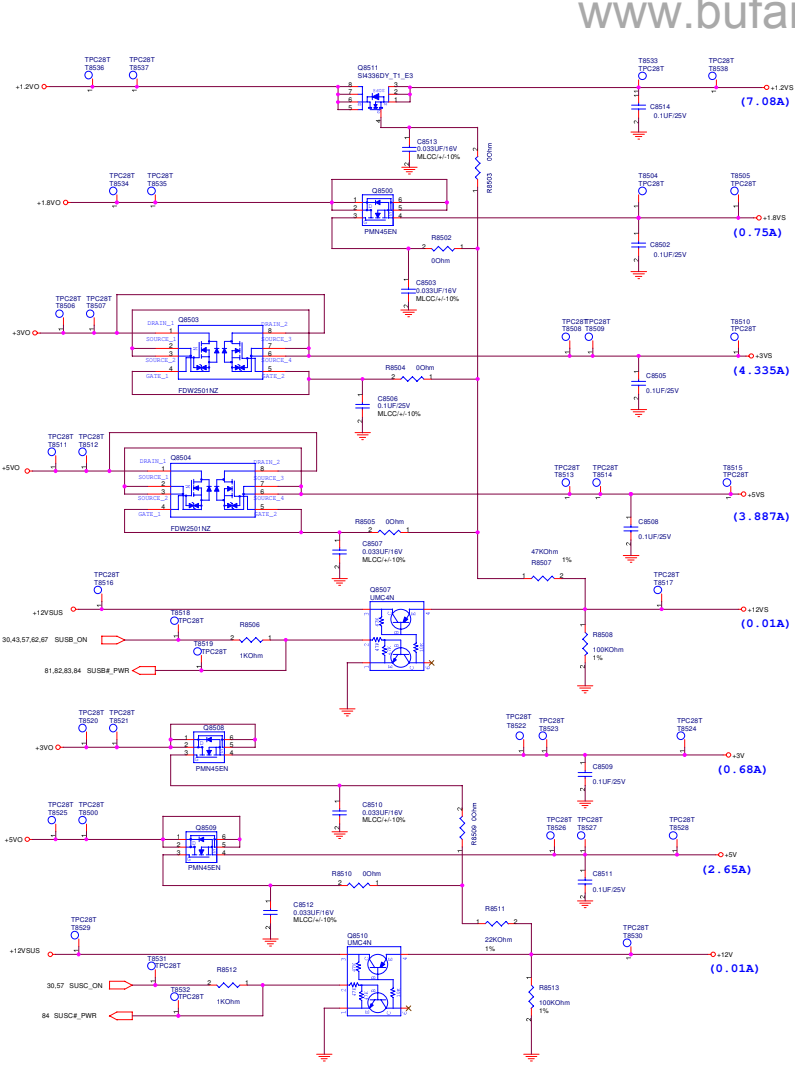
« Kennedy_Zhang »

ASUS		Title : POWER_IO_L00	
ASUSTECH	Project Name	Engineer: li-mei_chen	Rev
C	F5N		1.1
Date: 2011-07-26 20:00	Sheet: 61	of	68



ASUS		Title : POWER_IQ_D0R1	
ASUSTECH	Project Name	Engineer:	li-mei_chen
Custom	F5N		
Date: 11/11/09 2007	Sheet	84	of 88

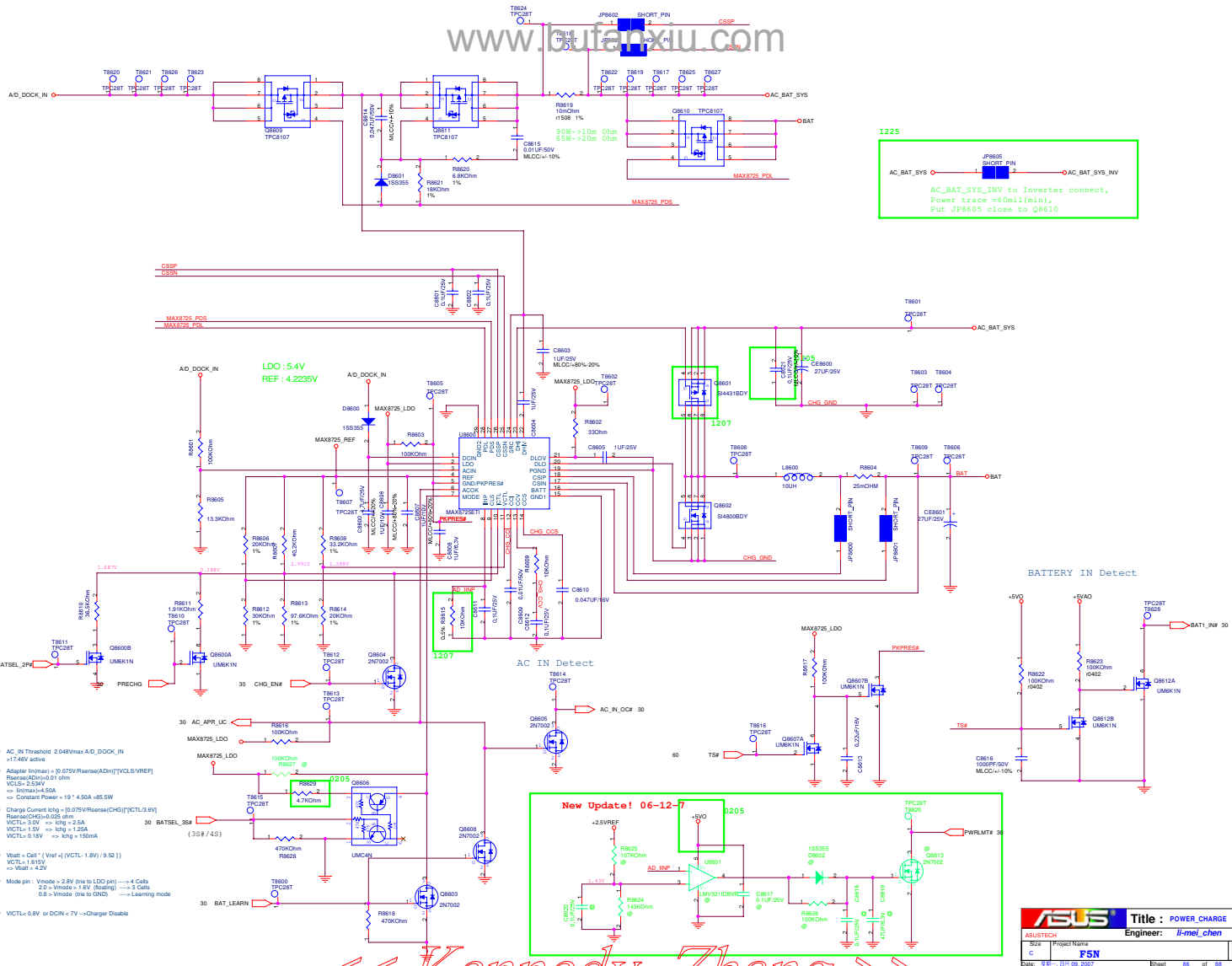
<< Kennedy_Zhang >>



+3VA	VSUS_ON	30.43.81.82
+3V0	CPU_VRON_PWR	80
	SUSBF_PWR	
	SUSCA_PWR	
	FOR TEST	

+3VA	15.30.46.56.62.67.82.83.84
+5V0	56.81.82.83.84.86
AC_BAT_SYS	AC_BAT_SYS 5.80.81.82.84.86
+VCORE	-VCORE 5.80
+5VAD	+5VAD 81.82.83.86
+3V0	81
+3V	30.34.43.46.53.57.61.62.63
+12VUS	+12VUS 81
+1.2V5_HT	+1.2V5_HT 3.5.10.15.57.82
+2.5V0	+2.5V0 83
+1.2VUS	+1.2VUS 12.16.82
+1.2V5	+1.2V5 11.14.16.57
+3V5	+3V5 3.7.8.10.11.12.13.14.15.16.30.36.37.43.44.45.46.50.51.53.56.57.62.67.80.82.87
+3V5S	+3V5S 1.2.14.15.16.30.33.34.43.53.56.57.67.81.82.84.87
+0.9V	+0.9V 5.57.84
+1.2V	+1.2V 37.52.57
+1.2V5	+1.2V5 37.45.46.57
+5V	+5V 3.7.40.43.46.52.57
+5V5	+5V5 15.30.36.37.45.50.51.56.57.80
+2.5V5	+2.5V5 3.57.83
+1.8V0	+1.8V0 84
+1.8V	+1.8V 3.5.7.8.9.10.15.57.82.84
+1.8V5	+1.8V5 12.57
BAT	BAT 60.86
+2.5VREF	+2.5VREF 82.83.86

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- AC_IN Threshold 2.048Vmax A/D_DOCK_IN
=> 1749V active
- Adapter In(max) = [0.075V/Rsense/A] * [VCL5/VREF]
Rsense=40mΩ/0.01 ohm
VCL5= 3.52V
=> In(max)=4.50A
- Charge Current kIq = [0.075V/Rsense/CHG] * [VCL3/VREF]
Rsense=40mΩ/0.02 ohm
VCL3= 3.0V => Iq = 2.5A
VCL4= 1.5V => Iq = 1.25A
VCL4= 0.18V => Iq = 150mA
- Vbat = Cell * [Vref - (VCL1 - Iq) / 9.52]
VCL1 = 1.815V
=> Vbat = 4.5V
- Mode pin : Vmode > 2.8V (High to LDO pin) => 4 Cells
2.8 > Vmode > 1.6V (Floating) => 3 Cells
0.5 > Vmode (pin to GND) => Learning mode
- VCL2= 0.6V or DCIN < 7V --> Charger Disable

ASUS		Title : POWER_CHARGE	
Rev	Project Name	Engineer	li-mei_chen
1	F5N		
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